High-Speed Constraint Values

and PCB Layout Methods

Charles Pfeil

3rd Edition

High-Speed Constraint Values and PCB Layout Methods

Charles Pfeil
Retired PCB Layout Software Architect

In the PCB industry for over 50 years, Charles has been a designer, owner of a service bureau, and had engineering management and product definition roles at Racal-Redac, ASI, Cadence, PADS, VeriBest, Mentor Graphics, and Altium.

Most of his career was at Mentor Graphics, where he was a software architect focused on the advanced development of PCB design tools. He was the original product architect of Expedition PCB, and an inventor of Team PCB, XtremePCB, XtremeAR, and the Sketch Router. He is also the author of *BGA Breakouts and Routing*.

3rd Edition

This edition includes updates regarding triplets from Daniel Beeker who originated the concept, and correcting the TPD values in this document and the calculator for differential pairs on stripline layers as identified by Liora Hertzog from Xsight. Changes are indicated with a line on the right side of the page.

For questions and comments:

Send an email to Charles Pfeil:
PCBconstraints@gmail.com

Table of Contents

Foreword

by Rick Hartley – Sr. Principal Engineer

When I began designing high-speed digital printed circuit boards, somewhere in the early 1990s, I soon realized that the days of tossing down components and routing however I pleased were gone. Welcome to the new era of controlled impedance, carefully thought-out parts placement and controlled routing. Over the past 30+ years, with the increase in circuit frequency and circuit speed, the task has become ever more challenging.

The most time-consuming part of planning and preparing a high-speed design remains to gather data and information on how to organize and place components, including line terminations, setting up and routing the many complex nets of the design, ensuring traces and their reference planes comply with the needed EMC, impedance, and timing requirements, all of which adds a massive amount of time to the design.

Today, one thing that helps the process is the availability of ECAD systems into which you can install the placement, routing, timing constraints, and the PCB stack-up, but you still have to go through the math and decision-making process to create reasonable constraint values. This remains one of the most time-consuming parts of the PCB design cycle.

If constraint values are not well-defined, the design will likely be compromised. Under-constraining can create a circuit that will not function as intended. Almost as bad is over-constraining, one of the worst mistakes a designer can make, as this potentially adds many hours to the design and, worse, adds cost to the bare PCB as layer count usually increases. I could fill a day with the horror stories I've seen due to the over-constraining of PCB designs.

This is where *High-Speed Constraint Values and PCB Layout Methods* comes into play. This fabulous treatise allows PCB designers and engineers to understand all the important constraints and determine their values in a fast and precise manner using the accompanying calculator. The calculator, in its own right, is marvelously designed and simple to use.

This book covers most aspects of high-speed design, items such as the importance of IC output rise time (edge rate), critical line length, the role of dielectric constant, impedance control, setting up constraint classes, reference planes, and signal returns, differential pair skew, including the impact of fiber weave, crosstalk, and trace corners, as well as via stubs and via impedance.

In addition to incorporating his wonderful ideas into this work, Charles includes information compiled from many sources, people such as Dr. Eric Bogatin, Dr. Howard Johnson, Lee Ritchey, Bill Hargin, Atar Mittal, Patrick Carrier, Randy Clemmons, Aliza Mizrachi, Michael Gay, Jeff Loyer, Richard Kunze, Mike Creeden, Dr. Doug Brooks, and Barry Olney, as well as a few items I put together over the years.

I only wish I had the luxury of this book and calculator many years ago. Oh, the wasted hours I could have saved!

Rick Hartley

March 2020

Preface

This book intends to provide PCB layout designers a relatively simple method to determine if a digital signal requires high-speed management and to offer a range of constraint values and layout methods to mitigate or eliminate the problems.

Critical length is the most important threshold that dictates when a signal requires high-speed management. When the total interconnect length for the signal exceeds the critical length, it becomes a distributed transmission line, and many high-speed effects must be mitigated or it will likely fail. The critical length value is derived from the edge rate and the dielectric constant of the materials.

This book can be considered a compendium of the PCB industry's thought about solving timing, crosstalk, and signal integrity problems in the PCB layout. I have relied on many high-speed design experts whose writings and presentations I have referenced.

I am grateful for the support of Mike Buetow and UP Media whose editing and publishing work has enabled this book to become available to the PCB industry.

The inspiration for this book comes from studying Rick Hartley's significant contributions to our industry regarding high-speed design. I highly recommend attending any of his seminars, watching his video presentations, and reading his articles and papers. I also want to thank Andy Haas and Randy Clemmons for their input on signal integrity issues and design practices as I worked on this project.

In the context of high-speed constraints, one difficulty for designers is figuring out what constraint values to use. In a perfect world, all ECAD systems would automatically fulfill every highly constrained rule without side effects; but in the real world, especially on a dense layout, design tradeoffs need to be made to avoid unnecessarily tight constraint values which can negatively impact the space, time, and cost requirements.

Constraint Value Calculator

After gaining an understanding of the high-speed concerns and constraint values in this book, the Constraint Value Calculator can be used to provide rules with appropriate constraint values. The calculator has options for the edge rate, dielectric constant, and the height between the layers to determine the constraint values.

On the next page is an image of the Constraint Value Calculator. The fields with a green background and white text are the variables that can be edited. Once those variables are defined for signals and the board environment they are in, the calculator will provide a range of values for constraints used to mitigate high-speed problems.

High-Speed Constraint Value Calculator

Edge Rate (ps)	300		Stripline Er =	4.10		Microstrip Er = 2.98	
	English						

Critical Length Values

	Problems Begin	Problems Definite	Problems Begin	Problems Definite
	Single Ended Nets			
Microstrip	512 mil	1025 mil	13.01 mm	26.03 mm
Stripline	437 mil	874 mil	11.10 mm	22.20 mm
	Differential Pairs			
Microstrip	466 mil	932 mil	11.84 mm	23.68 mm
Stripline	437 mil	874 mil	11.10 mm	22.20 mm

Differential Pair Within-Pair Length Match Tolerance

	Effective	Extreme	Effective	Extreme
Microstrip	± 615 mil	± 154 mil	± 15.62 mm	± 3.90 mm
Stripline	± 524 mil	± 131 mil	± 13.32 mm	± 3.33 mm

Differential Pair Phase Match - Parallel Distance ± Tolerance

	Effective	Extreme	Effective	Extreme
Microstrip	2049 ± 171 mil	512 ± 43 mil	52.05 ± 4.34 mm	13.01 ± 1.08 mm
Stripline	1748 ± 146 mil	437 ± 36 mil	44.41 ± 3.70 mm	11.10 ± 0.93 mm

Same Layer Trace Coupling - Parallel Distance / Clearance Values

Victim Height to Reference Plane	6	mil	0.15 mm				

(Use Victim Edge Rate)	Effective	Extreme	Effective	Extreme
	Single Ended Nets			
Microstrip	1025 / 24 mil	683 / 36 mil	26.03 / 0.61 mm	17.35 / 0.91 mm
Stripline	874 / 12 mil	583 / 24 mil	22.20 / 0.30 mm	14.80 / 0.61 mm
	Differential Pairs			
Microstrip	932 / 30 mil	622 / 42 mil	23.68 / 0.76 mm	15.79 / 1.07 mm
Stripline	874 / 24 mil	583 / 36 mil	22.20 / 0.61 mm	14.80 / 0.91 mm

Adjacent Layer Trace Coupling - Parallel Distance / Clearance Values

Height Between Agressor & Victim Layers	6	mil	0.15 mm
Victim Height to Reference Plane	4	mil	0.10 mm

(Use Victim Edge Rate)	Effective	Extreme	Effective	Extreme
	Single Ended Nets			
Microstrip	1025 / 15 mil	683 / 23 mil	26.03 / 0.38 mm	17.35 / 0.59 mm
Stripline	874 / 5 mil	583 / 15 mil	22.20 / 0.13 mm	14.80 / 0.38 mm
	Differential Pairs			
Microstrip	932 / 19 mil	622 / 27 mil	23.68 / 0.48 mm	15.79 / 0.69 mm
Stripline	874 / 15 mil	583 / 23 mil	22.20 / 0.38 mm	14.80 / 0.59 mm

Same Net Trace Coupling - Clearance Values

Route Height to Ref Plane or Width of 50 Ohm Trace	4	mil	0.10 mm

	Effective	Extreme	Effective	Extreme
Microstrip	16 mil	20 mil	0.41 mm	0.51 mm
Stripline	12 mil	16 mil	0.30 mm	0.41 mm

Max Stub Length Values for Vias & Traces

	Effective	Extreme	Effective	Extreme
	643 mil	429 mil	16.33 mm	10.89 mm

<div align="center">

CHAPTER 1

Introduction

</div>

High-Speed Concerns

Below is a list of the concerns addressed in this book by effective constraint values and layout methods:

Reference Planes
    Signal Return Path
    Differential Pair Stitch Vias

Timing Concerns
    Differential Pair Skew
    Differential Pair Fiberweave Skew
    Group Skew

Crosstalk & EMI Concerns
    Differential Pair Phase Mismatch
    Same Layer Coupling
    Adjacent Layer Coupling
    Same Net Coupling

Via Concerns
    Impedance
    Anti-Pad Size
    Via Stubs
    Nonfunctional Pads
    Differential Pair Via-Via Spacing

Routing Concerns
    Trace Stubs
    Trace Corners
    Differential Pair Split Around Objects

Critical Length

The third chapter describes a method to determine if a signal has exceeded its critical length from driver to receiver. At that length, the signal becomes a distributed length transmission line and must be managed properly, or it will become significantly degraded. The primary factor in determining the critical length is the edge rate.

Edge Rates

Throughout this book, constraint values are based on a portion of the signal edge rate; specifically, the rise time (Tr) and fall time (Tf). The faster the edge rate, the more likely the signal will have timing, crosstalk, and signal integrity problems. Also, the constraint values become tighter as the edge rate increases.

Technically, the edge rate is more akin to the slew rate rather than the rise and fall times. However, over many years, the PCB design industry has adopted edge rate as the term to express the faster of the rise and fall times. Edge rate in this book follows that legacy.

The abbreviation for rise time (Tr) is commonly used in equations and descriptions for the edge rate even though the fall time (Tf) may occasionally be faster.

10% to 90% vs. 20% - 80% - For many years, the rise and fall times were based on a 10% to 90% of the rising or falling edge. The PCB industry is moving to use 20% to 80% rise time (as with IBIS and Spice models[1]) to eliminate the usual distortion near the ends of the digital sine wave. Divide the 10% to 90% swing by 0.8/0.6 to convert it to a 20% to 80% swing.[2]
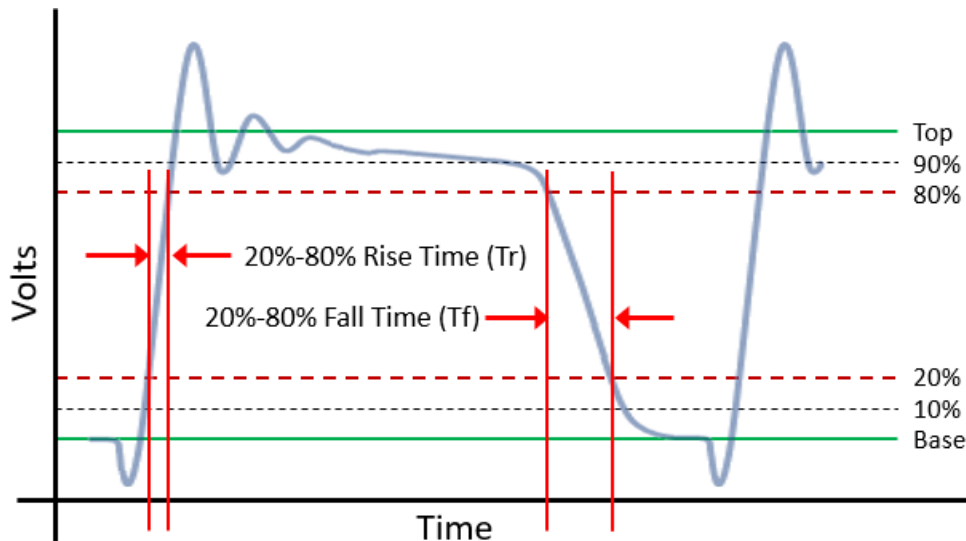

Figure 1.1: 20% to 80% Rise and Fall Times

How does one find the rise and fall times?

- **Specs and App Notes** - Although datasheets and application notes often do not include the rise and fall times, check them anyway, you may get lucky.

- **IBIS models** – These models are the best place to get rise and fall times.

    o Finding models: A good place to start the adventure to find IBIS models for your components is here: https://ibis.org/models/

- The IBIS models are provided by the device manufacturers and are often accessible only through an NDA.

o In this book, the need for simulation to verify the effectiveness of the constraints is mentioned over twenty-five times. To do that simulation, IBIS models will be required. Whoever will be doing the simulation should be encouraged to get the IBIS models early in the design cycle to determine the constraint values.

o The [PIN] section has the model assigned to each pin.

```
[PIN] signal_name  model_name  R_pin L_pin C_pin
AC14  RESET_IN_N    ddrmclk
```

o Each model is defined in its [Model] section by name. In each model is the [Ramp] section where rise and fall times are defined as dt_r and dt_f.

```
[Model] ddrmclk

[Ramp]
R_load = 50.00Ohm
|       typ                 min                 max
dV/dt_r 964.672mV/577.567ps 875.052mV/666.393ps 1.196V/273.717ps
dV/dt_f 875.701mV/663.089ps 767.445mV/759.584ps 1.196V/335.711ps
```

o Find the fastest of dt_r or dt_f in the max column. In this example, 273.717ps.

o Note that R_load provides the impedance for the driver which is the reference for impedance matching of the routing.

- **Tr from Bandwidth** - (Bogatin Rules of Thumb[1])
  o $\text{Tr[ps]} = \frac{350}{\text{BW [GHz]}}$ (Tr = the 10% to 90% rise time of a square wave in ps)

- **Tr from Data Rate** - Need to account for a multiplied rate as with DDR or QDR.
  o $\text{Tr[ps]} = \frac{140}{\text{DR [Gbps]}}$

Important High-Speed Methods

Before creating constraints and finding the values, a few things need to be done. Without them, a high-speed design is likely to fail no matter how well it is constrained.

- **Stackup & Reference Planes:** The materials and their thicknesses must be appropriate for the desired impedances. It is also essential to provide an effective reference plane adjacent to the high-speed signals.[6] Rick Hartley's video is excellent, especially when he talks about his enlightening conversation with Ralph Morrison on electric and magnetic fields, starting @ 10:11.[3]

- **Termination:** By terminating critical signals properly, the interconnect impedance at the receiver will match the impedance of the driver. This will minimize or eliminate significant reflections. It will also help for other high-speed problems[4,5]

- **Impedance Management:** All high-speed signals need to maintain a consistent impedance as specified in the datasheet, otherwise the reflections will degrade the signal quality. If the specified impedance for a net cannot be found, use 50Ω (Zo) for high-speed single-ended nets and 100Ω (Zdiff) for differential pairs.[6, 9, 10] The impedance of the driver, R_load, is in the IBIS file under [Ramp]

Range of Constraint Values

The values for each constraint are expressed in two categories.

1. **Effective Values:** These values are aligned with those recommended by Rick Hartley and Eric Bogatin and are excellent for very dense designs to avoid over-constraining. Effective means the values will sufficiently mitigate the problems.

2. **Extreme Values:** These values ensure that the problem is mitigated as much as possible by the constraint. However, using these values can over-constrain a design and may require more layers and more time to complete.

Choose an effective value, extreme value, or a value in between them, based on the situation with the design. It is important to avoid over-constraining.

In all cases, simulating the high-speed signals is the best way to determine if the design has been appropriately constrained.

Over-Constraining

Because our ECAD tools have become quite effective with interactive routing, tuning, and glossing algorithms, there is a tendency to set constraint values very tight. Indeed, the tools attempt to route and gloss with a zero-length tolerance and if it cannot fulfill that goal, it will still complete the task with the best tolerance it can. Setting very tight constraints may work in many circumstances; however, there can be side-effects when using values that are unnecessarily highly constrained.

- **Dense Boards**: The tuning required to match the length of a large bus to an unnecessarily tight tolerance can use a tremendous amount of space. This is especially true if the shortest route has significantly less length than the longest. Properly constraining the bus could require a lot less space.

- **Additional Layers**: If the space needed for over-constrained routing isn't available in the stackup, additional signal layers and reference planes will be required which will increase the cost.

- **Time to Route**: Even with highly automated routing tools, highly constrained routing in very dense areas with excessive tuning will often fail, requiring lots of manual routing and difficult editing which takes considerable time.

Dielectric Constant (ε_r)

In this book, the ε_r values used are for common FR-4 laminates:
- Stripline inner layers ε_r = 4.1
- Microstrip outer layers effective ε_r = 2.98

  o Due to the air, the microstrip effective ε_r is ≈ (0.64 ε_r + 0.36). This equation is approximate yet adequate for creating constraint values.

The ε_r value of 4.1 is used in this book because it is a typical dielectric constant for FR-4 materials. It is important to recognize that ε_r varies based on the frequency and the board material composition such as resin content, fiberglass weave, and thickness.[8]

When using high-speed laminates, for example from Isola[7], the ε_r value for stripline will be closer to 3.6, as also recommended by Sierra Circuits for high-speed materials.

Work with your fabricator and research the materials to determine what ε_r values should be used with the High-Speed Constraint Value Calculator and simulations.

Simulation

In the context of any particular digital design, there are factors not addressed in this book that can impact signal integrity, including but not limited to, stackup materials and configuration, power distribution, grounding methods, circuit technology, EMI, and fabrication practices. Every high-speed circuit should be validated using simulation and other methods to ensure the desired behavior before production.

References

1) Spice Models
   https://web.stanford.edu/class/ee133/handouts/general/spice_ref.pdf
   "Rise and Fall
   .MEAS TRAN rise TRIG V(1) VAL=.2 RISE=1 + TARG V(1) VAL=.8 RISE=1
   Gives the time it takes for node 1 to go from 20% to 80% of the maximum voltage (assuming a max voltage of 1V)"

IBIS Models
https://www.ti.com/lit/an/slyt413/slyt413.pdf?ts=1669906300870&ref_url=https%253A%252F%252Fwww.google.com%252F

"The range of the rise- and fall-time data is from 20 to 80% of the voltage-output signal."

2) Bonnie Baker, "IBIS model, Part 3," Copy/paste this link into a web browser, http://www.ti.com/lit/an/slyt413/slyt413.pdf

3) Eric Bogatin, "Rule of Thumb #1," https://www.colorado.edu/faculty/bogatin/rules-thumb

4) Rick Hartley, "Grounding to control EMI,"
Video, https://www.youtube.com/watch?v=ySuUZEjARPY
PDF, https://resources.altium.com/altiumlive-2018-summit/the-extreme-importance-of-pc-board-stack-up-rick-hartley

5) Dr. Howard Johnson, "Differential Termination,"
http://www.sigcon.com/Pubs/edn/DifferentialTermination.htm
Rick Hartley, "Control of Noise, EMI and SI," UP Media Group, PCB2Day workshop.

6) Lee Ritchey, "Designing a PCB Stackup,"
http://design.iconnect007.com/index.php/article/71690/lee-ritchey-designing-a-pcb-stackup-part-1/71693/?skin=design

7) Isola, "High-Speed Digital," https://www.isola-group.com/products/all-printed-circuit-materials/attributes/high-speed-digital/

8) Bill Hargin, Z-Zero, "PCB Stackup Design," PCB West 2018, pages 16,17,46.
Also check his website: https://www.z-zero.com/company/

9) Sierra Circuits, "Controlled Impedance Design Guide,"
https://www.protoexpress.com/controlled-impedance/design-guide/

10) Polar Instruments,
https://www.polarinstruments.com/support/cits/cits_index.html

CHAPTER 2

Setting Up Classes

Because the primary criteria for defining rule values for high-speed nets in this book is the edge rate, it is important to create net classes organized by edge rate.

1. **Create Net Classes by Edge Rate:** Organizing classes of nets based on their edge rates will allow them to be assigned to rules and the specific constraint value, based on the edge rate, to be applied to them.

2. **Max Length Rule:** For each edge rate class, create a max length rule with a value equal to its critical length, using the Constraint Value Calculator.
   - For example, if all the nets with an edge rate of 800 ps are put into a class named "Tr800ps" and a max length rule is created for that class, the value of the constraint can be assigned from the Constraint Value Calculator.

   - Some rules only apply to differential pairs and creating separate classes for them based on edge rate is convenient, such as "DP_Tr800ps".

3. **Placement:** Apply the max length rules on the netlines to help position the components so their length is less than the critical length.

4. **Routing:** After placement and before routing, duplicate the critical length classes and remove the signals whose Manhattan netline length does not exceed critical length; maybe name those classes with a "CL_" prefix to get, for example, "CL_Tr800ps".

   - Keep the original classes organized by edge rate and continue to check if any additional signals exceed their critical length (potentially during placement or route edits and length tuning) and add them to the appropriate edge rate class to manage their signal integrity.

Critical Length

CONCERN: When a signal exceeds its critical length, it becomes a distributed length transmission line that has effects that must be managed properly, or it will become significantly degraded. The critical length is the primary filter for determining if a net requires high-speed management.

- If a signal can be routed to less than its critical length, it will most likely not have the high-speed concerns described in this book which need to be mitigated.

- Critical length is exceeded when the time to propagate a conductor's length is greater than 1/4 of the signal rise or fall time, whichever is faster. This is when the problems begin.
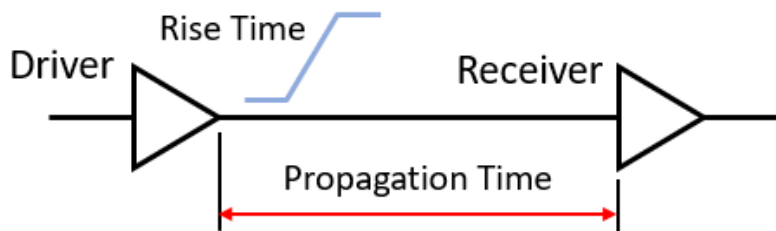
Figure 3.1: Propagation Time vs. Rise Time[2]

- If the total interconnect of the net is greater than its critical length, it must be managed with the constraints and/or methods as described in this book.
  - Total interconnect length includes pin-package, routing, and via-used lengths.

- Create max length constraints to flag nets exceeding their critical length.

Figures 3.2 and 3.3 present example critical length values for max length rules at which the signal "begins"[1,2] to have, or will "definitely"[3] have problems.

Use the High-Speed Constraint Calculator to get the critical length values for your specific edge rates and board materials.

Two charts are used, one for single-ended nets, Figure 3.2, and one for differential pairs, Figure 3.3. This is because on microstrip layers, the propagation delay (Tpd) of differential pairs is about 9% faster than single-ended nets, and the critical length for differential pairs is about 9% shorter.

Critical Length - Single-Ended Nets

	Edge Rate	English Units		Metric Units	
		Max Length Rule			
		Problems Begin (Tr/4)	Problems Definite (Tr/2)	Problems Begin (Tr/4)	Problems Definite (Tr/2)
MICROSTRIP Er = 2.98	2 ns	3.42 in	6.83 in	86.75 mm	174 mm
	1 ns	1.71 in	3.42 in	43.38 mm	86.75 mm
	700 ps	1.20 in	2.39 in	30.36 mm	60.73 mm
	500 ps	854 mil	1.71 in	21.69 mm	43.38 mm
	300 ps	512 mil	1.02 in	13.01 mm	26.03 mm
	100 ps	171 mil	342 mil	4.34 mm	8.68 mm
	50 ps	85 mil	171 mil	2.17 mm	4.34 mm
	25 ps	43 mil	85 mil	1.08 mm	2.17 mm
STRIPLINE Er = 4.10	2 ns	2.91 in	5.83 in	74.01 mm	148 mm
	1 ns	1.46 in	2.91 in	37.01 mm	74.01 mm
	700 ps	1.20 in	2.39 in	30.36 mm	60.73 mm
	500 ps	728 mil	1.46 in	18.50 mm	37.01 mm
	300 ps	437 mil	874 mil	11.10 mm	22.20 mm
	100 ps	146 mil	291 mil	3.70 mm	7.40 mm
	50 ps	73 mil	146 mil	1.85 mm	3.70 mm
	25 ps	36 mil	73 mil	0.93 mm	1.85 mm

Figure 3.2: Critical Length Values – Single-Ended Nets

Critical Length - Differential Pairs

	Edge Rate	English Units		Metric Units	
		Max Length Rule			
		Problems Begin (Tr/4)	Problems Definite (Tr/2)	Problems Begin (Tr/4)	Problems Definite (Tr/2)
MICROSTRIP Er = 2.98	2 ns	3.11 in	6.22 in	78.95 mm	158 mm
	1 ns	1.55 in	3.11 in	39.47 mm	78.95 mm
	700 ps	1.09 in	2.18 in	27.63 mm	55.26 mm
	500 ps	777 mil	1.55 in	19.74 mm	39.47 mm
	300 ps	466 mil	932 mil	11.84 mm	23.68 mm
	100 ps	155 mil	311 mil	3.95 mm	7.89 mm
	50 ps	78 mil	155 mil	1.97 mm	3.95 mm
	25 ps	39 mil	78 mil	0.99 mm	1.97 mm
STRIPLINE Er = 4.10	2 ns	2.91 in	5.83 in	74.01 mm	148 mm
	1 ns	1.46 in	2.91 in	37.01 mm	74.01 mm
	700 ps	1.20 in	2.39 in	30.36 mm	60.73 mm
	500 ps	728 mil	1.46 in	18.50 mm	37.01 mm
	300 ps	437 mil	874 mil	11.10 mm	22.20 mm
	100 ps	146 mil	291 mil	3.70 mm	7.40 mm
	50 ps	73 mil	146 mil	1.85 mm	3.70 mm
	25 ps	36 mil	73 mil	0.93 mm	1.85 mm

Figure 3.2: Critical Length Values – Differential Pair Nets

SOLUTION:

1. **Max Length Constraints**: Create constraints based on edge rates to identify critical length nets in the design by classes as described in Chapter 2.

2. **Reference Planes, Termination, Impedance**: See the Introduction in Chapter 1 to properly address these issues, as they are essential for critical length nets.

3. **Placement**: Use the max length rule as a filter during placement to discover which nets have exceeded their critical length. Then move the components closer to possibly prevent the nets from exceeding their critical length.

4. **Routing**: During routing, some nets may exceed their critical length due to excessive meandering. A max length rule would flag them.

5. **Simulation**: When working with high-speed signals, it is imperative to simulate to ensure timing, signal integrity (SI) and electromagnetic interference (EMI) problems are mitigated sufficiently to produce a layout that works as intended.

Equations

$$\text{Critical Length [in]} = \frac{\text{EdgeRate x LightSpeed}}{\sqrt{\text{DielectricConstant}}} = \frac{Tr \times C}{\sqrt{\mathcal{E}r}} = \frac{Tr \times 11.8\ [\text{in/ns}]}{\sqrt{\mathcal{E}r}}$$

Example: **Single-Ended Microstrip & Stripline, Differential Pair Stripline**,

Tr = 0.1 ns, Er = 4.1

$$\frac{0.1[\text{ns}] \times 11.8\ [\text{in/ns}]}{\sqrt{4.1}} = \frac{1.18\ [\text{in}]}{2.025} = 0.582[\text{in}] = 582[\text{mil}]$$

The single-ended critical length values in the chart are based on Tr/4 and Tr/2:

1. Problems begin @ Tr/4, for example, 582 mil /4 = 146 mil
2. Problems definite @ Tr/2, for example, 582 mil /2 = 291 mil

Example: **Differential Pair Microstrip**, Tr = 0.1 ns, Er = 4.1

(Tpd of differential pairs is about 9% faster than single-ended)

$$\frac{0.91 \times 0.1[\text{ns}] \times 11.8\ [\text{in/ns}]}{\sqrt{4.1}} = \frac{1.07\ [\text{in}]}{2.025} = 0.530[\text{in}] = 530[\text{mil}]$$

The differential pair critical length values in the chart are based on Tr/4 and Tr/2:

1. Problems begin @ Tr/4, for example, 530 mil /4 = 133 mil
2. Problems definite @ Tr/2, for example, 530 mil /2 = 265 mil

References

1) Lee Ritchey, "Right the First Time,"
   https://speedingedge.com/products/right-first-time/
   - Page 154, "Every signal path longer that ¼ TEL (Transition Electrical Length) has the potential to malfunction from overshoot."
2) Rick Hartley, "Control of Noise, EMI and SI," UP Media Group, PCB2Day workshop.
   - "Problems begin when the Time to Propagate a Conductor's Length is Greater than 1/4 of the Signal Rise or Fall Time."
3) Sierra Circuits, "PCB Transmission Line eBook," page 10,
   https://pages.protoexpress.com/pcb-transmission-line-ebook.html?utm_source=design%2Bguides&utm_medium=banner&utm_campaign=pcb%2Btl%2Bebook
   - "…the critical length lc is defined as the line length over which the signal propagation time is half of the fastest rise/fall time of the signal pulses.
4) Rick Hartley, "Grounding to control EMI,"
   Video, https://www.youtube.com/watch?v=ySuUZEjARPY
   PDF, https://resources.altium.com/altiumlive-2018-summit/the-extreme-importance-of-pc-board-stack-up-rick-hartley
5) Rick Hartley, "Control of Noise, EMI and SI," UP Media Group, PCB2Day workshop.

CHAPTER 4

Reference Planes: Signal Return Path

CONCERN: High-speed nets must have continuous coupling to an effective copper path to establish a reference for return currents or there will be significant EMI, crosstalk, and impedance problems. The reference can be either through a plane or trace shields.

- If the total interconnect length of the net is greater than the critical length, maintaining a signal return path with an adjacent reference plane is needed.
  - Total interconnect length includes pin-package, routing, and via-used lengths.

Rick Hartley's presentation at Altium Live, "The Extreme Importance of PC Board Stack-Up" delves into creating the best stackups for critical length nets.[1]

Dr. Bruce Archambeault's book, "PCB Design for Real-World EMI Control," is highly recommended by Rick Hartley for identifying and solving EMI problems.[4]

FIVE SPECIFIC CONCERNS AND SOLUTIONS:

1. Stackup and Reference Planes

CONCERN: If a critical length net is not routed on a layer adjacent to its reference plane layer, there will be significant EMI and crosstalk problems.

- If there is a routing layer between the signal and its reference plane, significant crosstalk will impact nets on the layer between them.

- If there are multiple layers between the critical length route and the reference plane, there may not even be a useful return path and the signal will fail.

SOLUTION:
1. **Reference Plane**: Needed on layer adjacent to critical length signals.

   - **EXTREMELY IMPORTANT:** The reference plane is best if it is a ground return, but it can be a voltage return ONLY if the plane is the voltage from which the signal was generated (for example, a 3.3v signal can reference a 3.3v plane), AND if the signal does not cross a split in this plane.

     Rick Hartley: "When the signal is referenced to the wrong voltage plane or

it crosses a split, the spreading of fields is severe, usually resulting in EMI issues. Since it seldom leads to SI issues, these EMI issues will not be identified in common SI simulations."

2. **Trace Shields**: If an adjacent reference plane is not available, as is common with double-sided boards and multilayer boards that don't have an ideal stackup, a ground trace is routed between the signal routes.[2]

   - The width of the ground trace should be the same as the signal traces.
   - Use the fabricators' minimum trace-trace clearance rule.
   - Make sure ground traces are connected to the ground at both ends.
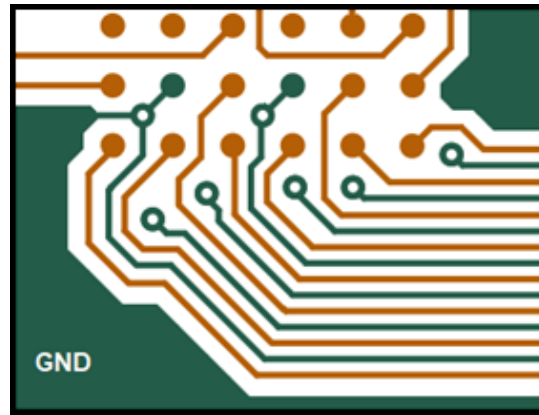
Figure 4.1: Trace Shield Routing

Using triplets for shielding transmission lines on a 2-layer design was first recommended by Daniel Beeker.[3] Figure 4.1 is from a Daniel Beeker presentation.
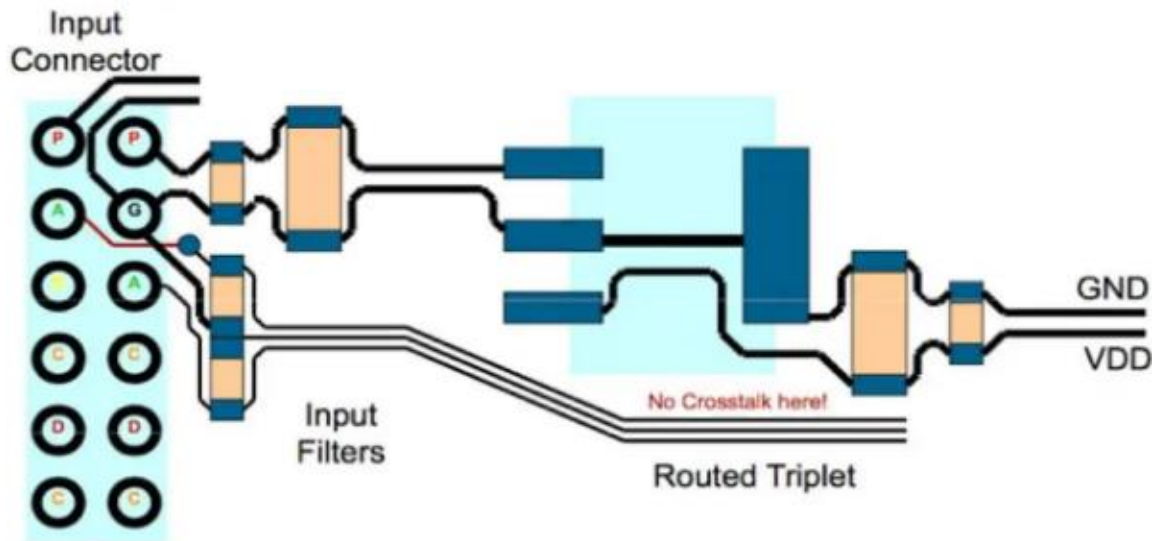
Figure 4.2: Triplets

2. Route Changing Layers

CONCERN: When a critical length signal changes layers, and if it does not maintain coupling to the same reference plane, the return path is degraded or eliminated.

SOLUTION:

1. **Opposite Side of Single Reference Plane**: When changing layers, route on opposite sides of one reference plane layer.
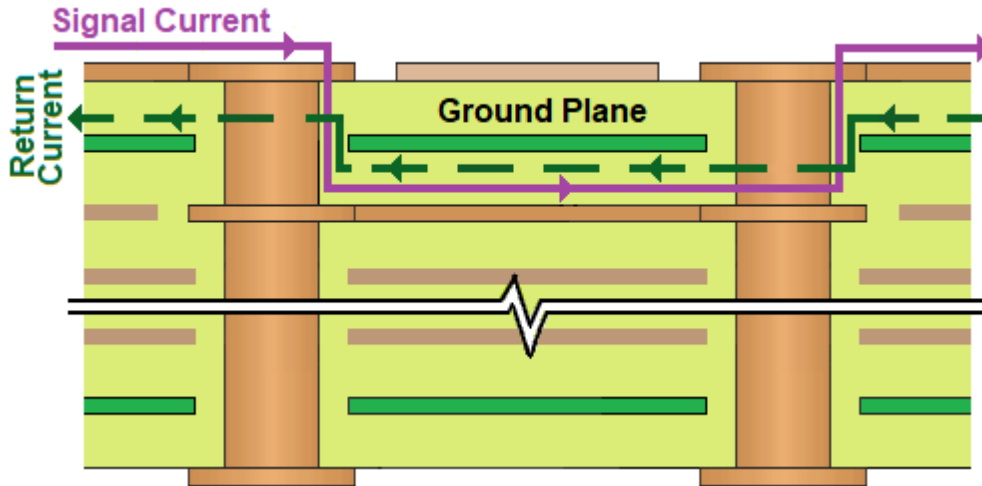
Figure 4.3: Route on Opposite Sides of Reference Plane Layer

- For critical length nets, create constraints that restrict their routing layers to those adjacent to reference planes.

2. **Couple to Multiple Reference Layers**: If the route must span multiple layers, make sure it is adjacent to another reference plane layer of the same net. Use a ground stitch via close to the net via to ensure the two planes are well connected.
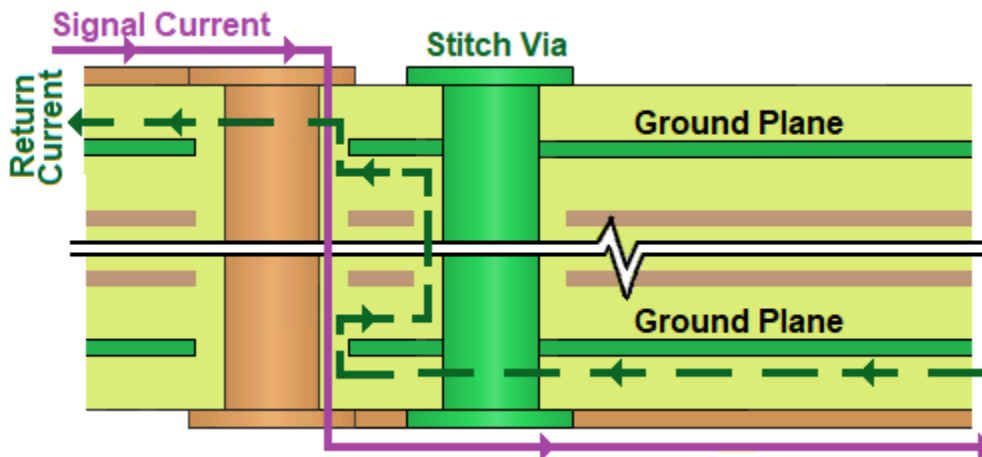
Figure 4.4: Stitch Via Connecting Ground Planes

3. Crossing Reference Plane Splits

CONCERN: When a critical length net crosses a plane split, the return path is either degraded or eliminated. This creates significant EMI and impedance discontinuities.

SOLUTION:

1. **Crossing Split Plane Rule**: Create a rule to prevent critical length nets from crossing any split in a plane. NEVER allow these nets to cross a plane split.

   - If the ECAD system supports a cross-plane split rule, include all critical length nets in a class and set the rule to prohibit the crossing.

2. **Route Obstruct**: If a rule is not available, put a route obstruct on each signal layer forcing the routes away from the split at a distance of 2x the trace width.

3. **Add Capacitor Across the Plane Split – Not Useful for High-Speed Signals:** Rick Hartley: "This method only works if the signals and all their harmonics are very low frequency, i.e. under 300 MHz. A signal with a 1.0 ns rising edge has harmonics to about 500 MHz, a 500 ps edge has harmonics to 1.0 GHz.[5]

4. Routing too Close to Edge of Reference Plane

CONCERN: When critical length nets are routed too close to the edge of their reference plane, the return path is affected, which can cause significant EMI and potentially an impedance discontinuity.

SOLUTION:

1. **Trace to Plane Edge Rule**: Use the rule to ensure the route is far enough away from the edge of the reference plane to maintain coupling.

   - Use a clearance to the edge of 2x the trace width (effective value), or 3x the trace width (extreme value).
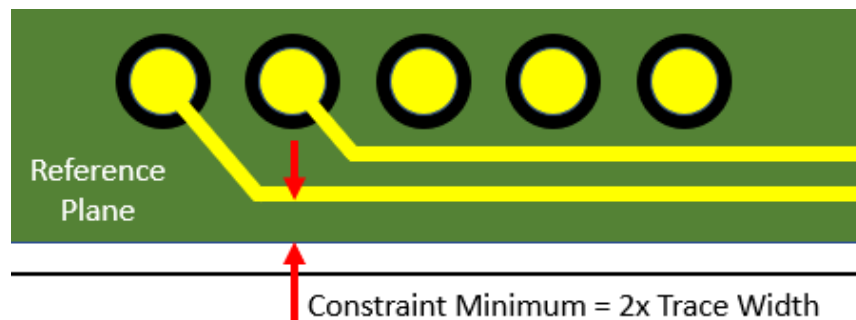
Figure 4.5: Trace to Plane Edge Constraint

2. **Route Obstruct**: If a rule is not available, add a route obstruct around the edge of the plane on each signal layer, forcing the routes away from the edge at 2x the trace width (effective value), or 3x the trace width (extreme value).
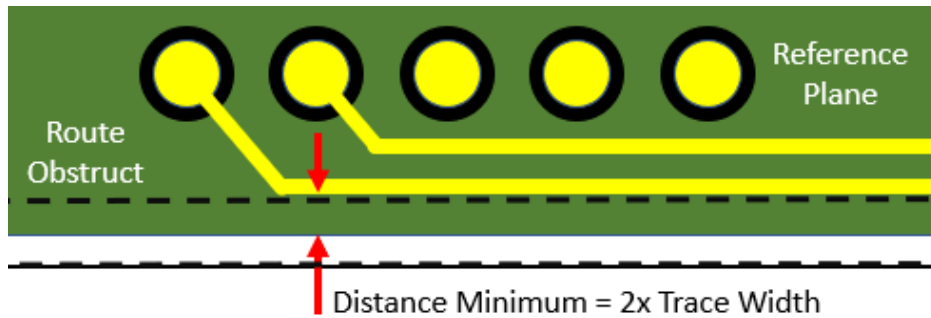
Figure 4.6: Using Route Obstruct

5. Crossing Anti-Pads and Holes in Reference Plane

CONCERN: When critical length nets cross over anti-pads in their reference plane, the return current is disturbed (causing EMI) and the impedance changes (causing reflections) as the route proceeds over the anti-pads.
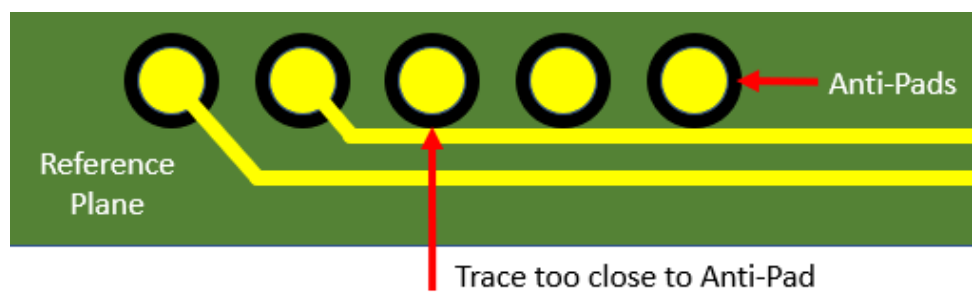

Figure 4.7: Critical Length Trace & Anti-Pads

SOLUTION: Ensure the route is far enough away from the anti-pads so the concern does not become a problem.

1. **Trace to Anti-Pad Rule**: Use the rule to ensure the critical route is far enough away from the anti-pad to prevent impedance discontinuities.

   - Use a clearance to the edge value of 1x the trace width (effective value), or 2x the trace width (extreme value).
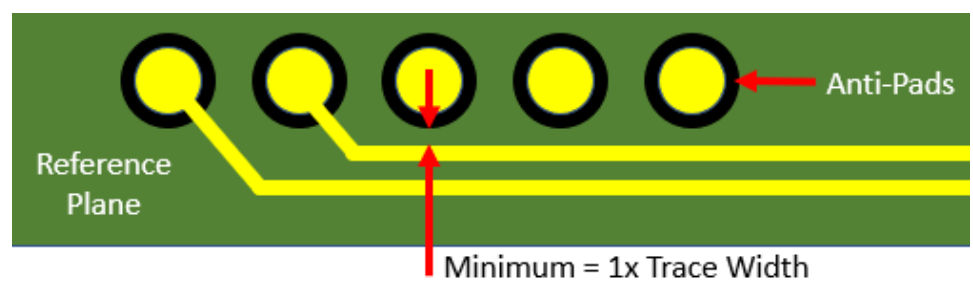
Figure 4.8: Trace to Anti-Pad Constraint

References

1) Rick Hartley, "Grounding to control EMI,"
   Video, https://www.youtube.com/watch?v=ySuUZEjARPY
   PDF, https://resources.altium.com/altiumlive-2018-summit/the-extreme-importance-of-pc-board-stack-up-rick-hartley

2) Rick Hartley, "Control of Noise, EMI and SI," UP Media Group, PCB2Day workshop.

3) Kenneth Watt, https://www.ednasia.com/design-pcbs-for-emi-part-2-basic-stack-up/

4) Patrick Carrier, Mentor Graphics, Signal Integrity Journal, "Design Rule Checks for High-Speed Design,"
   https://www.signalintegrityjournal.com/articles/577-design-rule-checks-for-high-speed-pcb-design

5) Dr. Bruce Archambeault, "PCB Design for Real-World EMI Control," page 72-77
   https://www.springer.com/gp/book/9781402071300.

CHAPTER 5

Reference Planes: Differential Pair Stitch Vias

CONCERN: The entirety of any critical length tightly coupled differential pair route must maintain the same reference (usually ground) from origination to termination otherwise there will be EMI issues and impedance discontinuities.

When a differential pair uses vias to traverse layers, there is a disruption of the return current. Stitch vias can normalize the return current and help prevent EMI issues in the power distribution network.

- If the total interconnect length for the differential pair is greater than its critical length, stitch vias should be used to ensure a proper return current.
  - Total interconnect length includes pin-package, routing, and via-used lengths.
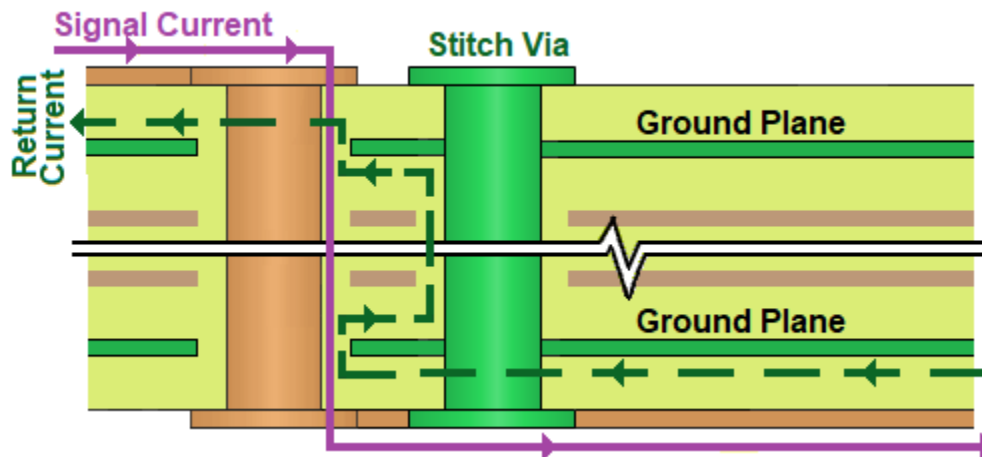
Figure 5.1: Reference Plane Coupling

- If the differential pair routing is on opposite sides of the same reference plane layer, coupling to ground is maintained and stitch vias are not required.

SOLUTIONS:

1. **Space Problems**: The primary difficulty when adding stitch vias is not having enough space, especially in fanout areas for pin array components and connectors.

   - Many FPGAs and ASICs today have ground pins next to high-speed differential pair pins. These ground fanouts can act like stitch vias inside the pin-array. For

example, Xilinx uses the Sparse Chevron pattern on its Virtex series in which every signal pin is adjacent to a ground return pin and their fanout vias are also stitch vias.

2. **Two Stitch Vias**: It is best to add two stitch vias by placing them symmetrically and equidistant from each differential pair via.
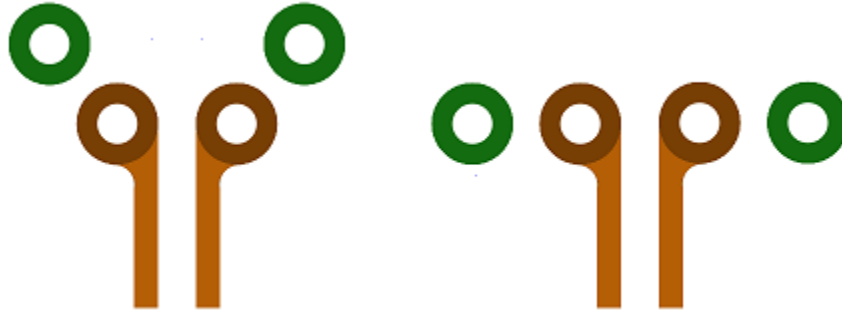
Figure 5.2: Dual Ground Stitch Vias

3. **One Stitch Via**: If adding one just stitch via, place it equidistant and as close as possible to the differential pair vias.

Figure 5.3: Single Ground Stitch Via

CHAPTER 6

Timing: Differential Pair Skew

CONCERN: The receiver of a differential pair signal reads the crossing event as one complement rises and the other falls. The skew budget is needed to avoid jitter introduced by the curved part of the edges.

- This concern is for all differential pairs, including those shorter than their critical length. However, note that the tolerance values based on the skew budgets are so large, only the ones with an extremely fast edge rate need this constraint.

- If on-die automatic within-pair skew compensation is available and applied successfully, the rule is not necessary.

- If needed, create within-pair match length constraints with a tolerance for differential pairs.

	Edge Rate	Skew Budget	English Units		Metric Units	
			Within-Pair Match Length: Tolerance			
			Effective Values	Extreme Values (1/4)	Effective Values	Extreme Values (1/4)
MICROSTRIP Er = 2.98	200 ps	± 60 ps	± 410 mil	± 102 mil	± 10.41 mm	± 2.60 mm
	100 ps	± 30 ps	± 205 mil	± 51 mil	± 5.21 mm	± 1.30 mm
	75 ps	± 23 ps	± 154 mil	± 38 mil	± 3.90 mm	± 0.98 mm
	50 ps	± 15 ps	± 102 mil	± 26 mil	± 2.60 mm	± 0.65 mm
	40 ps	± 12 ps	± 82 mil	± 20 mil	± 2.08 mm	± 0.52 mm
	30 ps	± 9 ps	± 61 mil	± 15 mil	± 1.56 mm	± 0.39 mm
	20 ps	± 6 ps	± 41 mil	± 10 mil	± 1.04 mm	± 0.26 mm
	10 ps	± 3 ps	± 20 mil	± 5 mil	± 0.52 mm	± 0.13 mm
STRIPLINE Er = 4.10	200 ps	± 60 ps	± 350 mil	± 87 mil	± 8.88 mm	± 2.22 mm
	100 ps	± 30 ps	± 175 mil	± 44 mil	± 4.44 mm	± 1.11 mm
	75 ps	± 23 ps	± 131 mil	± 33 mil	± 3.33 mm	± 0.83 mm
	50 ps	± 15 ps	± 87 mil	± 22 mil	± 2.22 mm	± 0.56 mm
	40 ps	± 12 ps	± 70 mil	± 17 mil	± 1.78 mm	± 0.44 mm
	30 ps	± 9 ps	± 52 mil	± 13 mil	± 1.33 mm	± 0.33 mm
	20 ps	± 6 ps	± 35 mil	± 9 mil	± 0.89 mm	± 0.22 mm
	10 ps	± 3 ps	± 17 mil	± 4 mil	± 0.44 mm	± 0.11 mm

Timing: Differential Within-Pair Skew

Figure 6.1: Within-Pair Tolerance

Notes

1. **Phase Matching:** Length matching, a timing concern, is different from phase matching (Chapter 9), which is a crosstalk and EMI concern. If phase matching is applied, the within-pair length matching rule is not needed because the phase matching will automatically fulfill the length matching requirement.

2. **Tolerances:** The tolerances in the chart are much greater than one would expect based on what we have been told to do in the past; for example, "Just use a tolerance of 5 mils for everything" or, "Make the lengths as close as possible." These other methods can result in over-constraining, which can create additional problems.[1]

3. **ECAD Rules:** If the routing is on both microstrip outer layers and stripline inner layers, and the ECAD system doesn't provide rules that account for the difference in propagation delay, use the tighter stripline layers tolerance for the microstrip layers tolerance.

SOLUTION:

1. **Within-Pair Match Length Tolerance Constraints**: If needed, create constraints based on edge rates for the differential pairs.

2. **Reference Planes, Termination, Impedance**: See the Introduction in Chapter 1 to properly address these issues as they are essential.

3. **Routing**: Route and tune the complements to match length within the tolerance.

   - This is length matching, not phase matching. The tuning bumps to match the lengths within tolerance may be added anywhere along the route path. Having said that, most designers will add the tuning bumps near the locations that cause the difference in length.
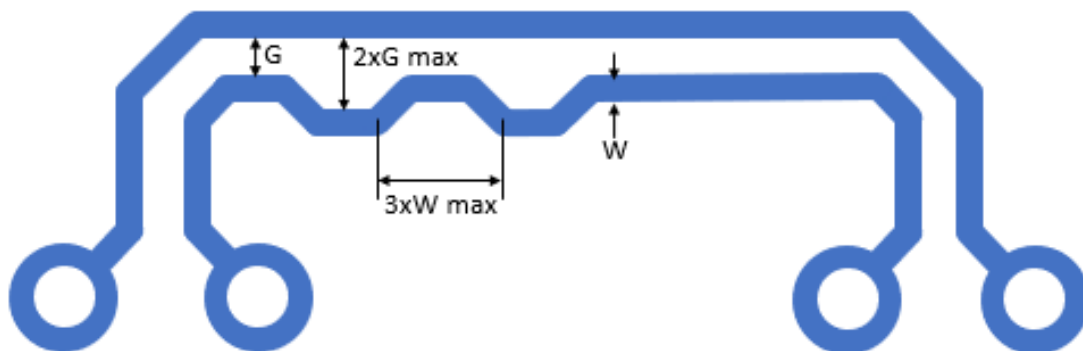
Figure 6.2: Length Match Differential Pair Complements

   - See Chapter 21 titled, "Length Matching Methods."

4. **Pad Exit**: When the traces exit the via or pin pads, they should converge at the gap spacing as soon as possible at equal length to minimize additional skew and help to maintain impedance. Some ECAD systems do this automatically.

Figure 6.3: Examples of "Converge as Soon as Possible with Equal Length"

5. **Simulation**: Simulate these differential pairs to ensure skew budgets are not exceeded.

Equations[1,2,3]

The skew budget is defined by the 20% - 80% region of the edge rate. Convert that skew budget into a length tolerance using the propagation velocity.

$$\text{Skew Budget } (SB) = 60\%\text{Tr} \qquad \text{Velocity}(V) = \frac{11.8\,[\text{in/ns}]}{\sqrt{\varepsilon_r} * 1000}$$

$$\text{Skew Length[mil]} = SB\,[\text{ps}] * V\,[\text{mil/ps}] \quad = \quad \frac{60\%Tr \text{ x } 11.8\,[\text{in/ns}]}{\sqrt{\varepsilon_r} * 1000}$$

$$\text{Skew Tolerance[mil]} = \text{Skew Length } / 2$$

For the tolerances, the skew length is based on the following ranges:

1. Effective values use Tr
2. Extreme values use Tr/4

References

1) Rick Hartley, "Control of Noise, EMI and SI," UP Media Group, PCB2Day workshop.
   - "Skew limits set by Tr/Tf (20% to 80% region) of the signal. Multiply fastest Tr/Tf by prop velocity in a PC Board [0.15mm (6 mils) / Ps in most dielectrics]. Results yield the skew budget."
2) Sierra Circuits, "PCB Transmission Line eBook," page 9, https://pages.protoexpress.com/pcb-transmission-line-ebook.html?utm_source=design%2Bguides&utm_medium=banner&utm_campaign=pcb%2Btl%2Bebook
3) Randy Clemmons, https://randy-clemmons.blogspot.com/2014/03/propagation-delay-tpd.html

CHAPTER 7

Timing: Differential Pair Fiberweave Skew

CONCERN: With differential pairs, if one complement runs over fiber and the other over resin for a long enough distance, there can be a significant difference in impedance for each signal. If so, the resulting difference in propagation delay may cause timing skew problems between the complements.[1]

- If the total interconnect length for each differential pair is greater than its critical length, the fiberweave skew needs to be mitigated.
    - Total interconnect length includes pin-package, routing, and via-used lengths.

- If on-die within-pair skew compensation is available and applied successfully, the fiberweave skew introduced may be eliminated; however, there may be significant reflections due to the impedance discontinuities.

Fiberweave skew contributes to the skew budget and unbalanced impedance discontinuities. Simulate to determine if there is a skew problem and address fiberweave skew only if necessary.

Different dielectric constant (Dk) between glass and resin

Diff Pairs Across Glass Weave

~21 mils

~21 mils

| 4% | Single End Impedance Variation | Negligible |
| 5.4% | Effective Dk Variation | Negligible |
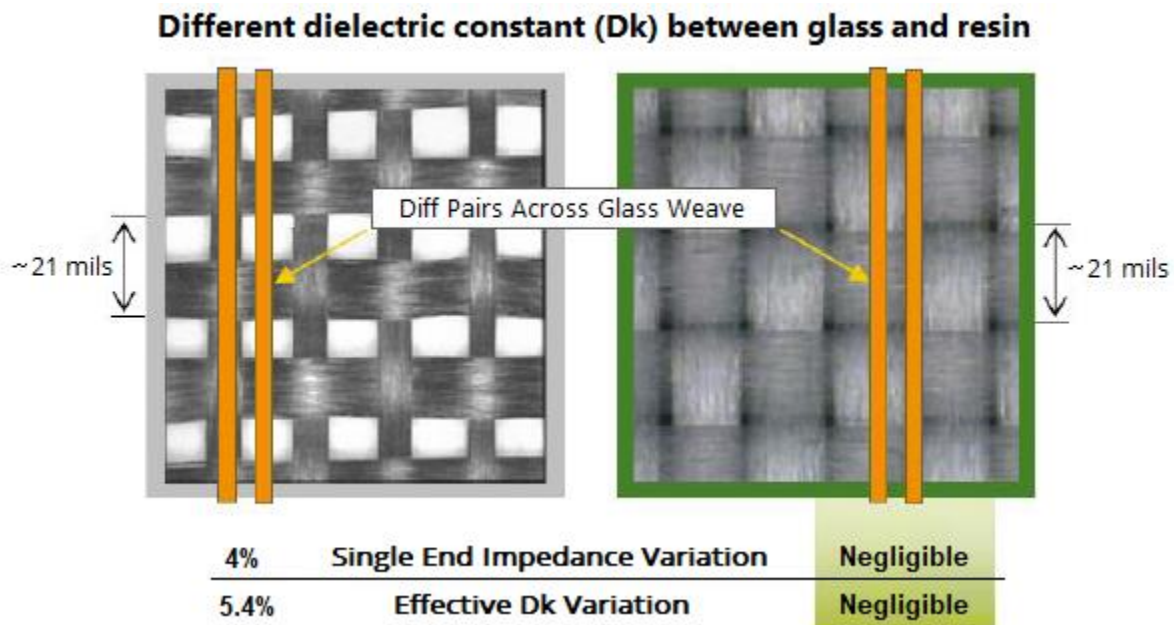
Figure 7.1: Fiberweave Effect on Differential Pairs[1]

The best analysis of the fiberweave skew was done by Jeff Loyer and the team at Intel and presented at DesignCon. To fully understand the problem and the simulations that resulted in their recommendations, see "Fiber Weave Effect: Practical Impact Analysis and Mitigation Strategies."[3]

The decision tree below shows common options and how to determine if any would be appropriate for the design. The ones highlighted in green are highly recommended. The others have undesirable side-effects.
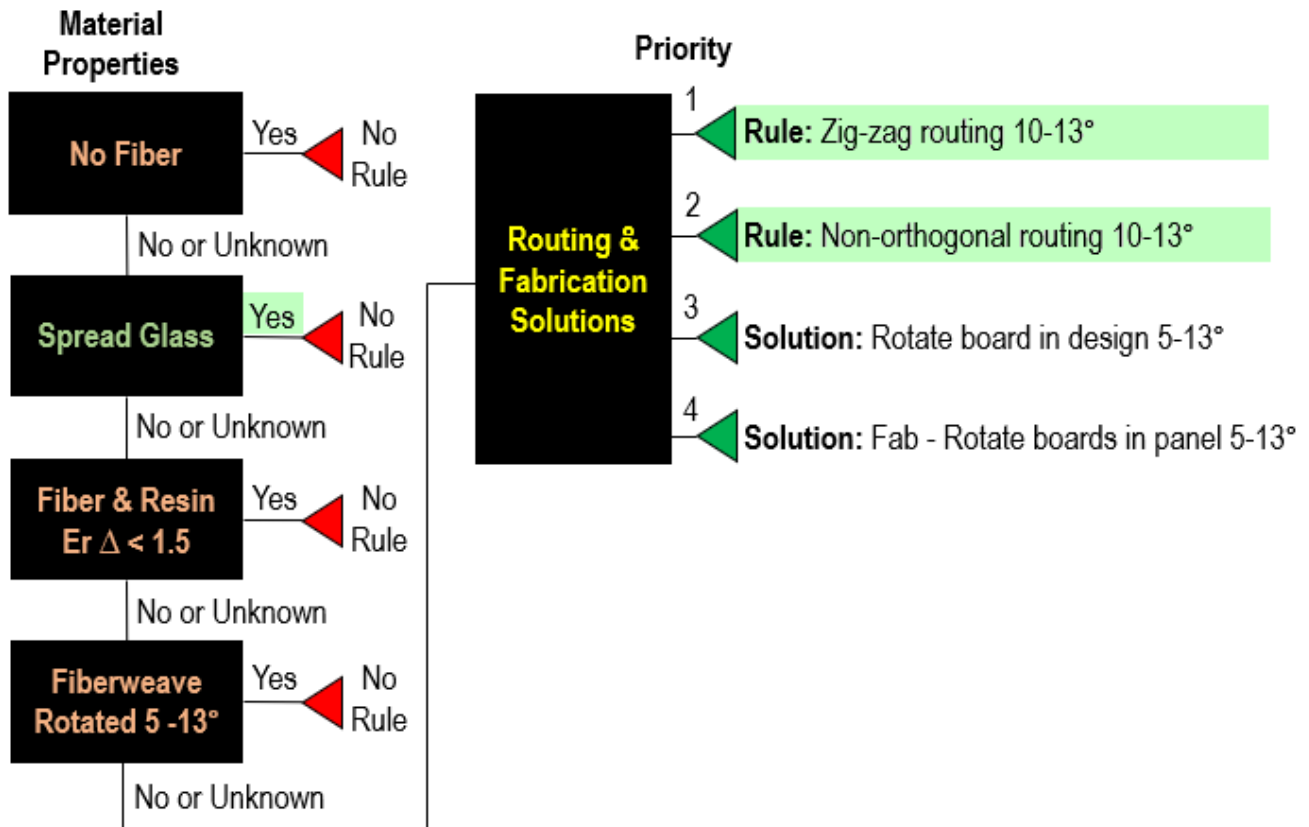
Figure 7.2: Fiberweave Skew

SOLUTION: There are multiple solutions as shown in the above figure.

1. **Few Critical Length Differential Pairs**: If the number of critical length differential pairs is not great and there is sufficient room on the design, zig-zag or non-orthogonal routing is the most effective solution.

2. **Many Critical Length Differential Pairs**: If there are a lot of critical length differential pairs and using zigzag or non-orthogonal routing creates space problems, the best solution is spread glass and use "normal" routing methods.

3. **Simulation**: Simulate to ensure timing requirements are met and the impedance discontinuities are insignificant.

Material Properties

1. **No Fiber**

   Without fiberglass weave, the impedance remains constant; however, the substrate will not be resistant to bending and breaking.

2. **Spread Glass[1,5]**

   This is considered the most effective solution, especially when the design is very dense with a lot of critical length differential pairs. The glass is spread to minimize the amount of resin-only exposure to the routing. Costs are getting lower as the demand increases. Isola examples: 1035MS, 1067MS, 1086Ms, 1078MS.
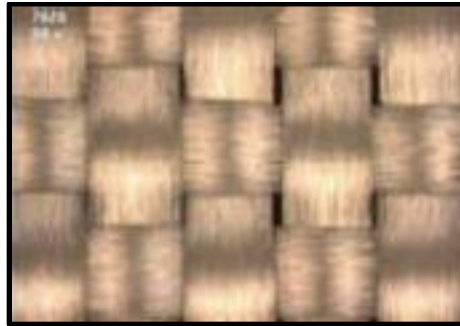
   Figure 7.3: 7628 Spread Glass Weave[2]

3. **Fiber and Resin ε_r Difference < 1.5**

   This could solve the problem; however, it is likely to be more expensive and doesn't work with extremely fast edge rates. Need to create test boards to determine if it will work.

4. **Fiberweave Rotated 5-13°**

   Currently, material suppliers are reluctant to do this. In the future, demand may motivate material suppliers to find a way to create inexpensive panels with the fiber rotated in the panel. Loyer[3] recommends a rotation of 10°.
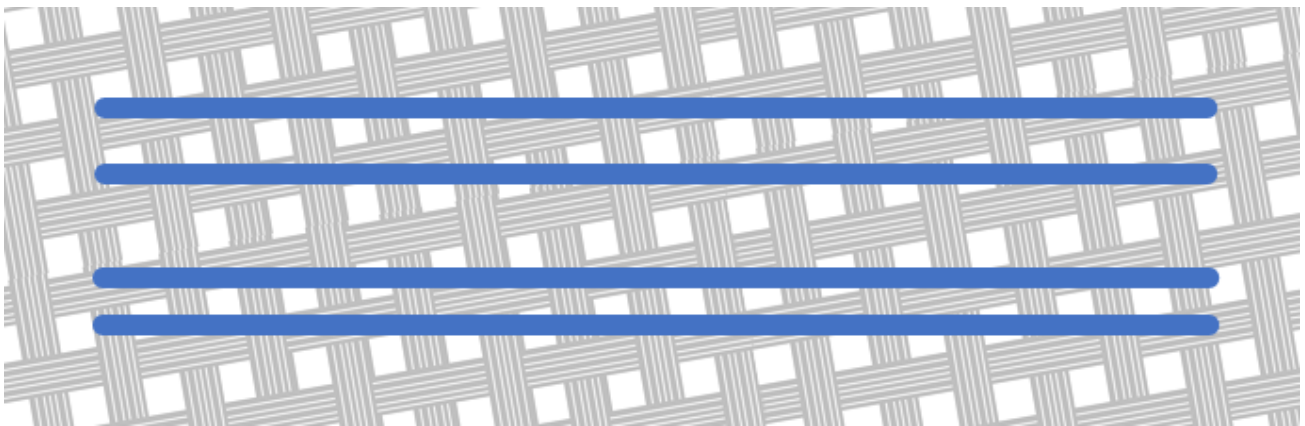
   Figure 7.4: Fiberweave in Panel Rotated 10°

Routing and Fabrication Solutions

1. **Rule: Zig-zag routing 10-13° [3,4]**
    Some ECAD layout tools have a zig-zag routing capability. This type of routing solves the problem; however, on a very dense board with a lot of differential pairs, there may not be room for it. This works well with a loose weave as in the 1080 material.
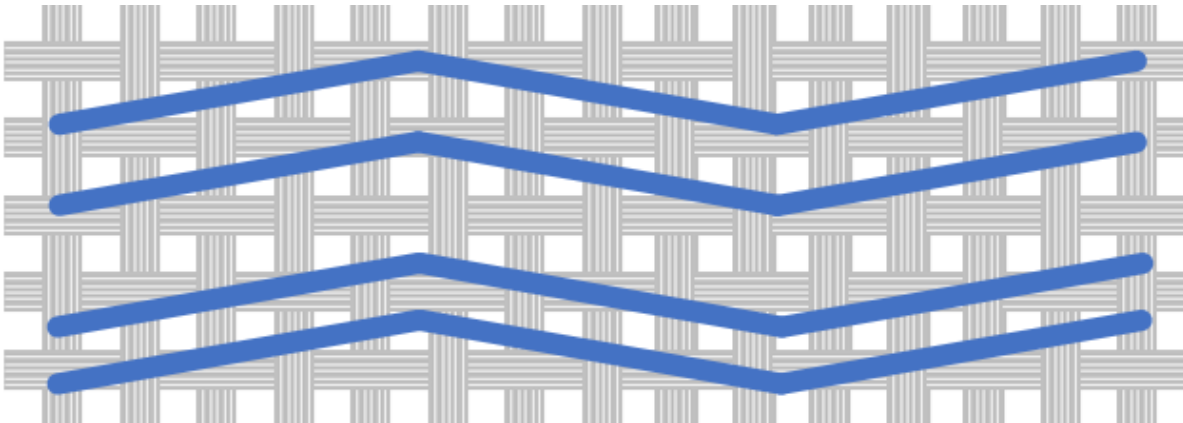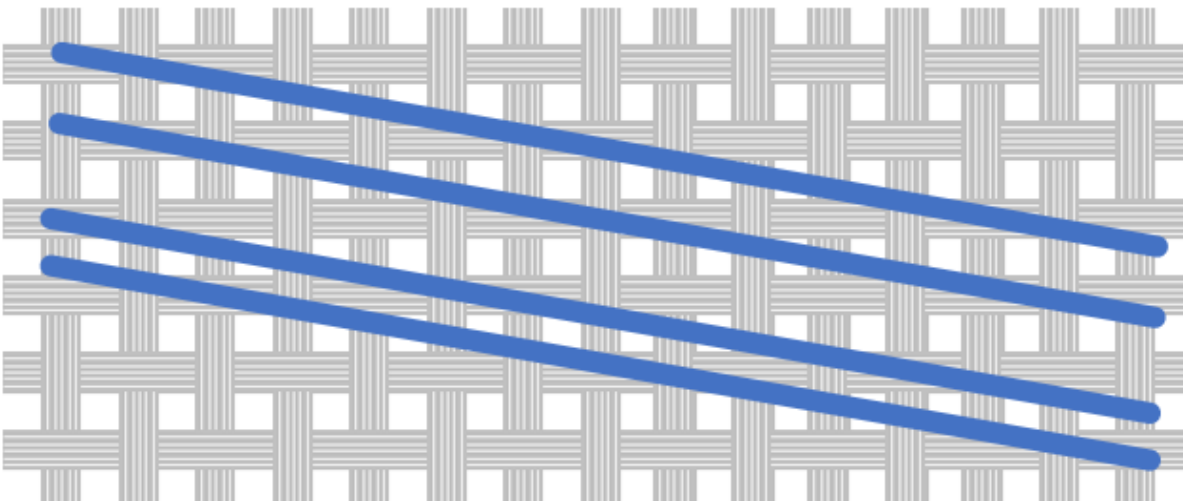

    Figure 7.5: Zig-zag Routing at 10°

2. **Rule: Non-orthogonal routing 10-13°**
    Some ECAD layout software has an angle offset capability. This type of routing solves the problem; however, on a very dense board with a lot of differential pairs, there may not be room for it. This works well with a loose weave as in 1080 material.

    Figure 7.6: Non-orthogonal routing at 10°

3. **Solution: Designer – Rotate board in design 5-13°**
    This will solve the problem but the number of boards on a panel will likely be reduced. This works well with a loose weave as in 1080 material.

The experts' opinions vary, but an angle between 5-13° should be sufficient to eliminate the fiberweave skew.

When using this method, make it noticeably clear to the fabricator that the boards must stay rotated as-is and they must not rotate the boards back to make them parallel to the weave.

4. **Solution: Fabricator – Rotate boards in panel 5-13°**
   This will solve the problem but the number of boards on a panel will likely be reduced. This works well with a loose weave as in 1080 material.

   The experts' opinions vary, but an angle between 5-13° should be sufficient to eliminate the fiberweave skew.

   When using this method, make it noticeably clear to the fabricator that the boards must be rotated in the panel.

References

1) Aliza Mizrachi, Orbotech, "Substrate Materials." Copy/paste link in browser to download paper, https://www.incoseil.org/check_download_nopass.php?forcedownload=1&file=files/Substrate__Materials.pdf&no_encrypt=true&dlpassword=14053

2) Michael J. Gay, Isola, "Advanced Material Selection," https://vdocuments.mx/advanced-material-selection-material-selection-ipc-designers-council-michael-j.html

3) Jeff Loyer, et al, "Fiberweave Effect, Practical Impact Analysis, and Mitigating Strategies," DesignCon 2007, https://docplayer.net/19727541-Fiber-weave-effect-practical-impact-analysis-and-mitigation-strategies.html

4) Caliber Interconnect Solutions, "Impact of Fiber Weave Effect on High-Speed Interconnects," https://caliberinterconnect.net/pdf/IMPACT_FIBER_WEAVE_%20EFFECT_ON_HIGHSPEEDINTERCONNECTS.pdf

5) Lee Ritchey, "High-Speed Design Class," video part 2, https://resources.altium.com/vidyard-all-players/lee-ritcheys-highspeed-design-class – starting at 52 minutes.

CHAPTER 8

Timing: Group Skew

CONCERN: A typical bus (or other collection of like signals) requires the same timing for all the signals within the skew margin. A constraint for the tolerance of the group is used to ensure the nets have the same interconnect length within tolerance maintaining the skew margin. The question is, "What should the tolerance be?"

Automatic Skew Adjustments

If skew compensation or automatic leveling is available, the skew is likely to be reduced to be within margin, and it won't be necessary to have a match length rule. For example, automatic leveling is common in DDR3 and later versions for the address, control and clock lines using fly-by topology.

Complexities

To paraphrase Rick Hartley, "There are many variables related to a bus with timing margins. Timing budgets are a function of clock frequency, setup and hold time, propagation delay within the ICs, etc. Timing budgets for an entire bus are considerably more complex than, for example, the skew budget for the two complements in a differential pair."

No attempt is made here in this book to calculate and provide the tolerances for group match length constraints. It is recommended to check the datasheet for the specific circuit to apply the timing margins and length tolerances.

SOLUTION:

1. **Match Length Constraints**: Use the match length tolerance as specified by the device vendor.

2. **Routing**: Route and tune to match length within the tolerance.

   - See Chapter 21 titled, "Length Matching Methods."

3. **Simulation**: Device vendors often recommend exceedingly tight match length tolerances. Simulate to determine if these are necessary with the intent of avoiding the negative layout effects of over-constraining.

CHAPTER 9

Crosstalk: Differential Pair Phase Mismatch

CONCERN: At fast edge rates, if the timing of the broad-side differential pair complements is not in phase throughout the interconnect, the signals are more susceptible to crosstalk and EMI.

- If the total interconnect length for the differential pair is greater than its critical length, the effects of phase mismatch must be mitigated.
  - Total interconnect length includes pin-package, routing, and via-used lengths.

- If the differential pairs are properly terminated, the need for phase matching can be eliminated: Simulate to determine if proper termination is successful. [1,2]

- If needed, create the phase matching constraints with distance and tolerance for differential pairs that exceed critical length to mitigate the crosstalk and EMI problems.

	Edge Rate	English Units		Metric Units	
		Phase Matching: Distance / Tolerance			
		Effective Values	Extreme Values (1/4)	Effective Values	Extreme Values (1/4)
MICROSTRIP Er = 2.98	200 ps	1366 / ± 114 mil	342 / ± 28 mil	34.70 / ± 2.89 mm	8.68 / ± 0.72 mm
	100 ps	683 / ± 57 mil	171 / ± 14 mil	17.35 / ± 1.45 mm	4.34 / ± 0.36 mm
	75 ps	512 / ± 43 mil	128 / ± 11 mil	13.01 / ± 1.08 mm	3.25 / ± 0.26 mm
	50 ps	342 / ± 28 mil	85 / ± 7 mil	8.68 / ± 0.72 mm	2.17 / ± 0.18 mm
	40 ps	273 / ± 23 mil	68 / ± 6 mil	6.94 / ± 0.58 mm	1.74 / ± 0.14 mm
	30 ps	205 / ± 17 mil	51 / ± 4 mil	5.21 / ± 0.43 mm	1.30 / ± 0.11 mm
	20 ps	137 / ± 11 mil	34 / ± 3 mil	3.47 / ± 0.29 mm	0.87 / ± 0.07 mm
	10 ps	68 / ± 6 mil	17 / ± 1 mil	1.74 / ± 0.14 mm	0.43 / ± 0.04 mm
STRIPLINE Er = 4.10	200 ps	1166 / ± 97 mil	291 / ± 24 mil	29.60 / ± 2.47 mm	7.40 / ± 0.62 mm
	100 ps	583 / ± 49 mil	146 / ± 12 mil	14.80 / ± 1.23 mm	3.70 / ± 0.31 mm
	75 ps	437 / ± 36 mil	109 / ± 9 mil	11.10 / ± 0.93 mm	2.78 / ± 0.22 mm
	50 ps	291 / ± 24 mil	73 / ± 6 mil	7.40 / ± 0.62 mm	1.85 / ± 0.15 mm
	40 ps	233 / ± 19 mil	58 / ± 5 mil	5.92 / ± 0.49 mm	1.48 / ± 0.12 mm
	30 ps	175 / ± 15 mil	44 / ± 4 mil	4.44 / ± 0.37 mm	1.11 / ± 0.09 mm
	20 ps	117 / ± 10 mil	29 / ± 2 mil	2.96 / ± 0.25 mm	0.74 / ± 0.06 mm
	10 ps	58 / ± 5 mil	15 / ± 1 mil	1.48 / ± 0.12 mm	0.37 / ± 0.03 mm

Figure 9.1: Phase Match Distance & Tolerance

- Phase matching is different from within-pair length matching which is a timing concern only at the receiver. If phase matching is applied to differential pairs, the within-pair length matching rule is automatically fulfilled.

Over-Constraining

Phase matching is a common cause of over-constraining. Note in Figure 9.1 how large the effective tolerance values are. Although it may be appropriate at extremely fast edge rates, it tends to be used unnecessarily with many high-speed nets.

This note from Rick Hartley illustrates how phase matching has its limits,

"In reality, the perfect phase matching of a differential pair is nearly impossible. Fiber weave issues run amuck with 106 and 1080 glass, but they also exist, to a lesser degree, in all fiberglass weave. All glass styles have knuckles and valleys, even the tightly woven glass. Routing two lines, side by side, over those hills and valleys will create some level of phase skew and there is little you can do about it. When I was in Telecom, we fretted that problem, not because of timing, but because of EMI with our first 10 Gbit system. We were not concerned about timing; we knew we could match our skew budget easily enough. We were concerned about EMI. That's when I first read Howard Johnson's termination scheme, with 2 resistors and a capacitor. We started using that arrangement to terminate all diff pairs and, by all appearances, seem to have eliminated the issue. That termination scheme eliminates the common mode current in one of the lines."

SOLUTION:

1. **Termination**: Apply Howard Johnson's scheme to manage the EMI concern.[2]

2. **Reference Planes, Impedance**: See the Introduction in Chapter 1 to properly address these issues as they are essential for critical length nets.

3. **Phase Match Length / Tolerance Constraints**: If needed, create constraints with distance and tolerance based on edge rates for differential pairs greater than their critical length.

4. **Routing and Tuning**:
   - For each distance, add phase bumps on the shorter route to meet the tolerance – preferably close to the location where the phase mismatch occurs.
   - When an impedance discontinuity occurs in the interconnect, such as a via, pin, gap or width change, ensure the phase matching is near that location.
   - See Chapter 21 titled, "Length Matching Methods."

5. **Simulation**: To ensure crosstalk and EMI effects are sufficiently mitigated, simulate all the differential pairs that have phase matching.
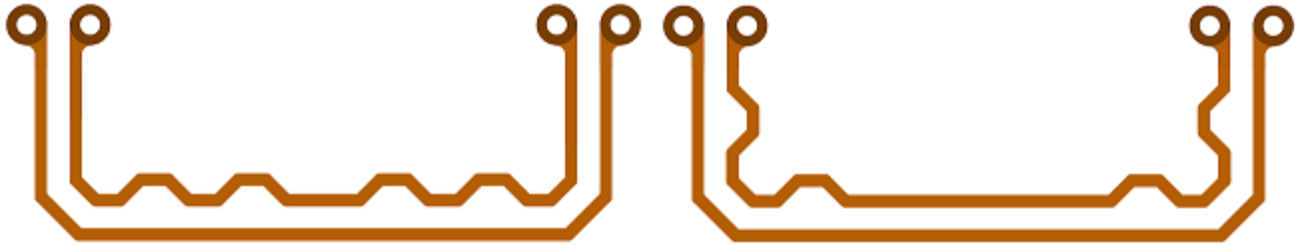
Phase Bumps

Figure 9.2: Adding Phase Bumps

If phase matching must be done and the tolerance is small, phase bump tuning can be done anywhere before the distance increment or at an impedance discontinuity. However, it is preferred to add the phase bumps near the location of the mismatch.
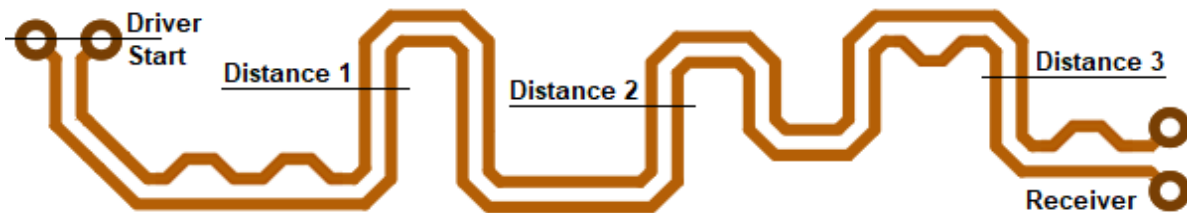

Figure 9.3: Phase Matching Technique

In the above figure, note that phase bumps not required between "Distance 1" and "Distance 2" because an even number of bends in the serpentines results in an equal distance for both compliments.

Equations

The distance equation for phase matching is the same as the one used for critical length.

$$\text{Distance [mil]} = \frac{\text{EdgeRate x LightSpeed}}{\sqrt{\text{DielectricConstant}} * 1000} = \frac{Tr \text{ x } C}{\sqrt{\varepsilon_r} * 1000} = \frac{Tr \text{ x } 11.8 \text{ [in/ns]}}{\sqrt{\varepsilon_r} * 1000}$$

$$\text{Tolerance [mil]} = \frac{\text{Distance}}{12}$$

For the phase match parallel distance, use the following ranges:

1. Effective values use Tr
2. Extreme values use Tr/4

References

1) Rick Hartley, "Control of Noise, EMI and SI," UP Media Group, PCB2Day workshop.
2) Dr. Howard Johnson, "Differential Termination,"
    http://www.sigcon.com/Pubs/edn/DifferentialTermination.htm

CHAPTER
10

Crosstalk: Same Layer Coupling

CONCERN: When an aggressor net (usually a clock or other periodic signal) is routed too close and parallel to victim nets on the same layer, inductive crosstalk can occur with electromagnetic field coupling, and the victim signals can be significantly distorted with the backward reflection of the wave. It becomes a problem when the aggressor and victim are parallel past the crosstalk critical length (also called critical parallel length) and are spaced too close.

- If the total interconnect length of the victim is greater than its critical length, the crosstalk must be mitigated or eliminated.
  - Total interconnect length includes pin-package, routing, and via-used lengths.

- Create the same layer parallelism constraints with a max distance of parallelism between the aggressor and victim using a clearance value that effectively separates them, thus minimizing the crosstalk. The clearance value is a multiple of the height of the victim from its reference plane.

Most of the data presented for the constraint values are based on Rick Hartley's "Control of Noise, EMI and SI " presentation. [1]
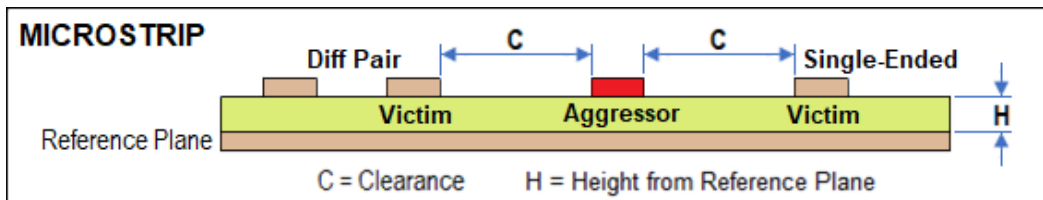
Figure 10.1: Same Layer Coupling – Microstrip
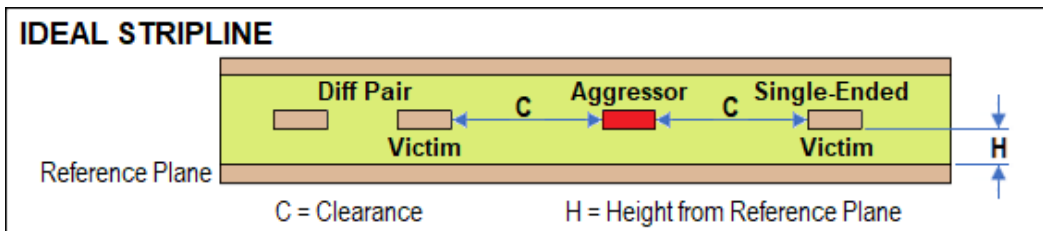
Figure 10.2: Same Layer Coupling – Stripline

Crosstalk: Same Layer Coupling - Single-Ended Nets

Victim Edge Rate	English Units		Metric Units	
	Critical Parallel Length / Clearance			
	Effective Values	Extreme Values	Effective Values	Extreme Values
MICROSTRIP Er = 2.98				
1 ns	3.42 in / 2H	2.28 in / 4H	86.75 mm / 2H	57.84 mm / 4H
500 ps	1.71 in / 2H	1.14 in / 4H	43.38 mm / 2H	28.92 mm / 4H
350 ps	1.20 in / 4H	797 mil / 6H	30.36 mm / 4H	20.24 mm / 6H
250 ps	854 mil / 4H	569 mil / 6H	21.69 mm / 4H	14.46 mm / 6H
100 ps	342 mil / 4H	228 mil / 6H	8.68 mm / 4H	5.78 mm / 6H
50 ps	171 mil / 4H	114 mil / 6H	4.34 mm / 4H	2.89 mm / 6H
25 ps	85 mil / 4H	57 mil / 6H	2.17 mm / 4H	1.45 mm / 6H
10 ps	34 mil / 4H	23 mil / 6H	0.87 mm / 4H	0.58 mm / 6H
STRIPLINE Er = 4.10				
1 ns	2.91 in / 2H	1.94 in / 4H	74.01 mm / 2H	0.05 mm / 4H
500 ps	1.46 in / 2H	0.97 in / 4H	37.01 mm / 2H	0.02 mm / 4H
350 ps	1.02 in / 4H	680 mil / 6H	25.90 mm / 4H	17.27 mm / 6H
250 ps	728 mil / 4H	486 mil / 6H	18.50 mm / 4H	12.34 mm / 6H
100 ps	291 mil / 4H	194 mil / 6H	7.40 mm / 4H	4.93 mm / 6H
50 ps	146 mil / 4H	97 mil / 6H	3.70 mm / 4H	2.47 mm / 6H
25 ps	73 mil / 4H	49 mil / 6H	1.85 mm / 4H	1.23 mm / 6H
10 ps	29 mil / 4H	19 mil / 6H	0.74 mm / 4H	0.49 mm / 6H

Clearance value = Multiple of the height (H) to reference plane

Figure 10.3: Same Layer Coupling – Single-Ended Nets

Crosstalk: Same Layer Coupling - Differential Pairs

Victim Edge Rate	English Units		Metric Units	
	Critical Parallel Length / Clearance			
	Effective Values	Extreme Values	Effective Values	Extreme Values
MICROSTRIP Er = 2.98				
1 ns	3.11 in / 2H	2.28 in / 4H	78.95 mm / 2H	57.84 mm / 4H
500 ps	1.55 in / 2H	1.14 in / 4H	39.47 mm / 2H	28.92 mm / 4H
350 ps	1.09 in / 4H	797 mil / 6H	27.63 mm / 4H	20.24 mm / 6H
250 ps	777 mil / 4H	569 mil / 6H	19.74 mm / 4H	14.46 mm / 6H
100 ps	311 mil / 4H	228 mil / 6H	7.89 mm / 4H	5.78 mm / 6H
50 ps	155 mil / 4H	114 mil / 6H	3.95 mm / 4H	2.89 mm / 6H
25 ps	78 mil / 4H	57 mil / 6H	1.97 mm / 4H	1.45 mm / 6H
10 ps	31 mil / 4H	23 mil / 6H	0.79 mm / 4H	0.58 mm / 6H
STRIPLINE Er = 4.10				
1 ns	2.91 in / 2H	1.94 in / 4H	74.01 mm / 2H	0.05 mm / 4H
500 ps	1.46 in / 2H	0.97 in / 4H	37.01 mm / 2H	0.02 mm / 4H
350 ps	1.02 in / 4H	680 mil / 6H	25.90 mm / 4H	17.27 mm / 6H
250 ps	728 mil / 4H	486 mil / 6H	18.50 mm / 4H	12.34 mm / 6H
100 ps	291 mil / 4H	194 mil / 6H	7.40 mm / 4H	4.93 mm / 6H
50 ps	146 mil / 4H	97 mil / 6H	3.70 mm / 4H	2.47 mm / 6H
25 ps	73 mil / 4H	49 mil / 6H	1.85 mm / 4H	1.23 mm / 6H
10 ps	29 mil / 4H	19 mil / 6H	0.74 mm / 4H	0.49 mm / 6H

Clearance value = Multiple of the height (H) to reference plane

Figure 10.4: Same Layer Coupling – Differential Pairs

On microstrip layers, differential pairs are about 9% faster than single-ended nets and therefore the critical parallel length for differential pairs is 91% of single-ended nets. On stripline layers, the difference is insignificant.

The clearance is a factor relative to the trace distance to the reference plane. The smaller the distance to the reference plane, the smaller the clearance value will be.

If precise calculations are desired to determine the crosstalk coefficient and coupled voltage, see the reference for EEWeb[2], otherwise, the clearance value can be derived from the charts above and the Constraint Value Calculator. The amount of crosstalk should be kept to less than 5%.

Broadside Differential Pairs – Crosstalk is not equal on tightly coupled differential pair complements routed together on the same layer. The aggressor's crosstalk is significantly greater on the closest compliment and common mode rejection will not occur; therefore, it is necessary to increase the clearance between the closest compliment and the aggressor to mitigate the crosstalk.

SOLUTION:

1. **Same Layer Crosstalk Constraints**: Create parallelism constraints (parallel distance, clearance) for critical length nets using victim and aggressor classes.

   - Victims: Use the same classes created for critical length nets organized by edge rates as defined in Chapter 3.

   - Aggressors: Create a class of aggressor nets, named "Aggressors" which includes all clock and other periodic signals that have exceeded their critical length (Tr/4) as defined in Chapter 3.

     o If potential aggressors are not routed, use the netline Manhattan Length to determine if the net is greater than its critical length.

2. **Reference Planes, Termination, and Impedance**: See the Introduction, Chapter 1, to properly address these issues as they are essential for critical length nets.

   - Keep the impedance of the routes 50 ohms or less.[3] At higher impedances, the clearance needs to be greater so the extreme values will work, but simulation is needed to validate the effectiveness.

3. **Routing Techniques**:

   - Use Ideal Stripline Layers - Preferably route critical victims on ideal stripline layers where they are routed between reference planes. This should effectively eliminate forward crosstalk problems and enable the best management of backward crosstalk.

- Different Technologies - Avoid routing different technologies parallel to each other. These crosstalk mitigation methods work best for victims and aggressors of the same technology.

- Eliminate Parallelism - Looking at the cover of this book, there are obvious instances of the routing with jogs and clearance changes. Initially, I was concerned that it wasn't the kind of uniform and consistent routing that many of us designers love to achieve. Then I remembered a discussion I had with Jeff Loyer when I was working with our development team on some routing tools.

  I showed him some results in which the routes were rather chaotic, like this book cover, not running parallel to each other as many designers would route manually. I told him the glossing algorithm was not working very well and we were working to correct that, and he said, "No! This is perfect, you are reducing the parallel length and helping to prevent crosstalk."

  Using this method can prevent surpassing the critical parallel length. Other constraints like length matching and max length also must be managed.

Figure 10.5: Eliminating Parallelism with Jogs and Clearance Changes.

4. **Simulation**: To ensure crosstalk effects have been sufficiently mitigated, simulate all the victims.

Equations

The crosstalk critical length (or critical parallel length) equation is the same equation used for critical length with the Tr factor modified slightly.

Parallel Distance (mil) =

$$\frac{EdgeRate \times LightSpeed}{\sqrt{DielectricConstant} * 1000} = \frac{Tr \times C}{\sqrt{\varepsilon_r} * 1000} = \frac{Tr \times 11.8 \,[in/ns]}{\sqrt{\varepsilon_r} * 1000}$$

Parallel Distance in chart uses modified Tr:

1. Effective values use Tr/2
2. Extreme values use Tr/3

Tabbed Routing

If you would like an interesting read about an Intel method to reduce or eliminate forward crosstalk and manage impedance, check out these links:

- Richard Kunze, "Crosstalk Mitigation and Impedance Management Using Tabbed Lines,"
  https://www.intel.com/content/www/us/en/processors/xeon/crosstalk-mitigation-impedance-management-paper.html
- Cadence, Allegro, "Tabbed Routing,"
  https://community.cadence.com/cadence_blogs_8/b/pcb/posts/next-generation-hs-routing-with-tabbed-routing

References

1) Rick Hartley, "Control of Noise, EMI and SI," UP Media Group, PCB2Day workshop.
2) EEWeb, Crosstalk Calculators,
   https://www.eeweb.com/tools/microstrip-crosstalk
   https://www.eeweb.com/tools/stripline-crosstalk
3) Lee Ritchey, "High-Speed Design Class," video part 4, at 17 minutes.
   https://resources.altium.com/vidyard-all-players/lee-ritcheys-highspeed-design-class

CHAPTER 11

Crosstalk: Adjacent Layer Coupling

CONCERN: When an aggressor net (usually a clock or other periodic signal) is routed too close and parallel to victim nets on adjacent layers, capacitive crosstalk occurs with electromagnetic field coupling, and the victim signals can be significantly distorted. It becomes a problem when the aggressor and victim are parallel past the crosstalk critical length (also called critical parallel length) and are spaced too close.

- If the total interconnect length of the victim is greater than its critical length, the crosstalk must be mitigated or eliminated.
  - Total interconnect length includes pin-package, routing, and via-used lengths.

- Create adjacent layer parallelism constraints with a max distance of parallelism between the aggressor and victim using a clearance value that effectively separates them, thus minimizing the crosstalk. The clearance value is a multiple of the height of the victim from its reference plane.

Most of the information presented for this concern is based on Rick Hartley's "Control of Noise, EMI and SI " presentation.[1]
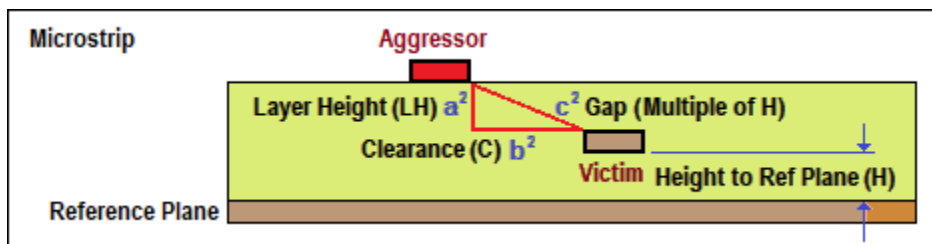
Figure 11.1: Adjacent Layer Coupling – Microstrip
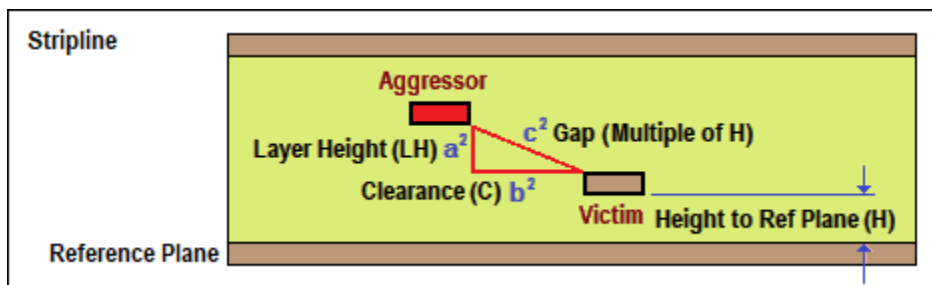
Figure 11.2: Adjacent Layer Coupling – Stripline

Crosstalk: Adjacent Layer Coupling - Single-Ended Nets

Victim Edge Rate	English Units		Metric Units	
	Critical Parallel Length / Clearance			
	Effective Values	Extreme Values	Effective Values	Extreme Values
MICROSTRIP Er = 2.98				
1 ns	3.42 in / 1.7H	2.28 in / 3.9H	86.75 mm / 1.7H	57.84 mm / 3.9H
500 ps	1.71 in / 1.7H	1.14 in / 3.9H	43.38 mm / 1.7H	28.92 mm / 3.9H
350 ps	1.20 in / 3.9H	797 mil / 5.9H	30.36 mm / 3.9H	20.24 mm / 5.9H
250 ps	854 mil / 3.9H	569 mil / 5.9H	21.69 mm / 3.9H	14.46 mm / 5.9H
100 ps	342 mil / 3.9H	228 mil / 5.9H	8.68 mm / 3.9H	5.78 mm / 5.9H
50 ps	171 mil / 3.9H	114 mil / 5.9H	4.34 mm / 3.9H	2.89 mm / 5.9H
25 ps	85 mil / 3.9H	57 mil / 5.9H	2.17 mm / 3.9H	1.45 mm / 5.9H
10 ps	34 mil / 3.9H	23 mil / 5.9H	0.87 mm / 3.9H	0.58 mm / 5.9H
STRIPLINE Er = 4.10				
1 ns	2.91 in / 1.7H	1.94 in / 3.9H	74.01 mm / 1.7H	0.05 mm / 3.9H
500 ps	1.46 in / 1.7H	0.97 in / 3.9H	37.01 mm / 1.7H	0.02 mm / 3.9H
350 ps	1.02 in / 3.9H	680 mil / 5.9H	25.90 mm / 3.9H	17.27 mm / 5.9H
250 ps	728 mil / 3.9H	486 mil / 5.9H	18.50 mm / 3.9H	12.34 mm / 5.9H
100 ps	291 mil / 3.9H	194 mil / 5.9H	7.40 mm / 3.9H	4.93 mm / 5.9H
50 ps	146 mil / 3.9H	97 mil / 5.9H	3.70 mm / 3.9H	2.47 mm / 5.9H
25 ps	73 mil / 3.9H	49 mil / 5.9H	1.85 mm / 3.9H	1.23 mm / 5.9H
10 ps	29 mil / 3.9H	19 mil / 5.9H	0.74 mm / 3.9H	0.49 mm / 5.9H
Clearance value = Multiple of the height (H) to reference plane				

Figure 11.3: Adjacent Layer Coupling – Single-Ended Nets

Crosstalk: Adjacent Layer Coupling - Differential Pairs

Victim Edge Rate	English Units		Metric Units	
	Critical Parallel Length / Clearance			
	Effective Values	Extreme Values	Effective Values	Extreme Values
MICROSTRIP Er = 2.98				
1 ns	3.11 in / 1.7H	2.28 in / 3.9H	78.95 mm / 1.7H	57.84 mm / 3.9H
500 ps	1.55 in / 1.7H	1.14 in / 3.9H	39.47 mm / 1.7H	28.92 mm / 3.9H
350 ps	1.09 in / 3.9H	797 mil / 5.9H	27.63 mm / 3.9H	20.24 mm / 5.9H
250 ps	777 mil / 3.9H	569 mil / 5.9H	19.74 mm / 3.9H	14.46 mm / 5.9H
100 ps	311 mil / 3.9H	228 mil / 5.9H	7.89 mm / 3.9H	5.78 mm / 5.9H
50 ps	155 mil / 3.9H	114 mil / 5.9H	3.95 mm / 3.9H	2.89 mm / 5.9H
25 ps	78 mil / 3.9H	57 mil / 5.9H	1.97 mm / 3.9H	1.45 mm / 5.9H
10 ps	31 mil / 3.9H	23 mil / 5.9H	0.79 mm / 3.9H	0.58 mm / 5.9H
STRIPLINE Er = 4.10				
1 ns	2.91 in / 1.7H	1.94 in / 3.9H	74.01 mm / 1.7H	0.05 mm / 3.9H
500 ps	1.46 in / 1.7H	0.97 in / 3.9H	37.01 mm / 1.7H	0.02 mm / 3.9H
350 ps	1.02 in / 3.9H	680 mil / 5.9H	25.90 mm / 3.9H	17.27 mm / 5.9H
250 ps	728 mil / 3.9H	486 mil / 5.9H	18.50 mm / 3.9H	12.34 mm / 5.9H
100 ps	291 mil / 3.9H	194 mil / 5.9H	7.40 mm / 3.9H	4.93 mm / 5.9H
50 ps	146 mil / 3.9H	97 mil / 5.9H	3.70 mm / 3.9H	2.47 mm / 5.9H
25 ps	73 mil / 3.9H	49 mil / 5.9H	1.85 mm / 3.9H	1.23 mm / 5.9H
10 ps	29 mil / 3.9H	19 mil / 5.9H	0.74 mm / 3.9H	0.49 mm / 5.9H
Clearance value = Multiple of the height (H) to reference plane				

Figure 11.4: Adjacent Layer Coupling – Differential Pairs

Differential pairs are about 9% faster than single-ended nets on microstrip layers and therefore the critical parallel length for differential pairs is 91% of single-ended nets.

The difference between the clearance values for the same layer coupling and adjacent layer coupling is small with most stackups. To get accurate results, use the Constraint Value Calculator.

SOLUTION: Manage the potential crosstalk with these methods:

1. **Adjacent Layer Orientation:** If adjacent layers are routed one in X and one in the Y direction, the opportunity significant for parallelism can be eliminated.

2. **Adjacent Layer Crosstalk Constraints**: Create adjacent layer parallelism constraints (parallel distance, clearance) using the victim and aggressor classes. Depending on the ECAD system, these constraints may be the same as the parallelism constraints for the same layer coupling. In that case, the parallelism constraints are applied to the same layer or in the z-axis.

   - Victims: Use the same classes created for nets organized by edge rates as defined in Chapters 2 and 3.

   - Aggressors: Create a class of aggressor nets, named "Aggressors," which includes all clock and other periodic signals that have exceeded their critical length (problems begin Tr/4) as defined in Chapter 3.

     o If potential aggressors are not routed, use the netline Manhattan Length to determine if the net is greater than its critical length.

3. **Reference Planes, Termination, and Impedance**: See the Introduction, Chapter 1, to properly address these issues as they are essential for critical length nets.

   - Keep impedance of the routes 50 ohms or less.[3] At higher impedances, the clearance needs to be greater and the extreme values should work.

4. **Routing Techniques**:

   - Preferably route critical victims on ideal stripline layers near a reference plane. This will mitigate the possibility of adjacent layer crosstalk.

   - Avoid routing different technologies parallel to each other. These crosstalk mitigation methods best apply to victims and aggressors of the same technology.

5. **Simulation**: To ensure crosstalk effects have been sufficiently mitigated, simulate all the victims.

Equations

The crosstalk critical length (or critical parallel length) equation is the same equation used for critical length with the Tr factor modified slightly.

Parallel Distance (mil) =

$$\frac{\text{EdgeRate x LightSpeed}}{\sqrt{\text{DielectricConstant}}*1000} = \frac{Tr \text{ x } C}{\sqrt{\mathcal{E}r}*1000} = \frac{Tr \text{ x } 11.8\,[\text{in/ns}]}{\sqrt{\mathcal{E}r}*1000}$$

Parallel distance in the charts use modified Tr:

1. Effective values use Tr/2
2. Extreme values use Tr/3

For the adjacent layer coupling clearance value, most ECAD systems have rules that use a clearance (C) value as a multiple of the height to the reference plane (H), similar to the method for the same layer coupling clearance.

However, a more accurate value would be to apply the multiple of the reference plane height (H) to the gap distance in the z-axis as shown in Figure 11.5.
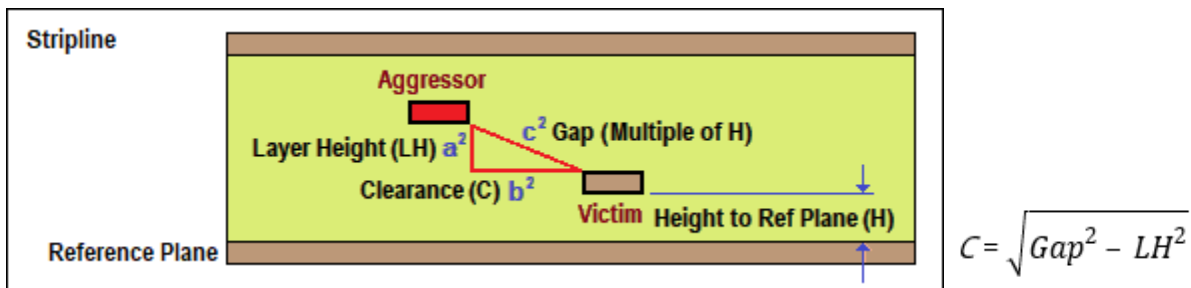
Figure 11.5: Pythagoras Theorem

This is the value that the charts above and the Constraint Value Calculator will provide and then (C) will be slightly smaller than the gap which is a multiple of the height (H).

References

1) Rick Hartley, "Control of Noise, EMI and SI," UP Media Group, PCB2Day workshop.
2) Doug Brooks, "Crosstalk, Part 2: How Loud is Your Crosstalk?" https://www.ultracad.com/articles/crosstlk.pdf
3) Lee Ritchey, "High-Speed Design Class" video part 4, (choose 4/4 in the upper left of the video) starts about 17 minutes, https://resources.altium.com/vidyard-all-players/lee-ritcheys-highspeed-design-class

CHAPTER 12

Crosstalk: Same Net Coupling

CONCERN: The most common occurrence of the same net coupling comes from tuning for length adjustment. If the same net space between two segments is inadequate, the added length could effectively be ignored because the electromagnetic wave would couple across, rather than follow, the serpentine route waveguide.

- If the total interconnect length of the victim is greater than its critical length, the opportunity for self-coupling must be eliminated.
  - Total interconnect length includes pin-package, routing, and via-used lengths.

- Create the same net clearance constraints for nets exceeding their critical length.

The orange line is an approximation showing a significant portion of the electromagnetic wave path coupling into a same net segment when the clearance is inadequate.

Figure 12.1: Single-Ended Clearance Inadequate, and Then Good When Spread
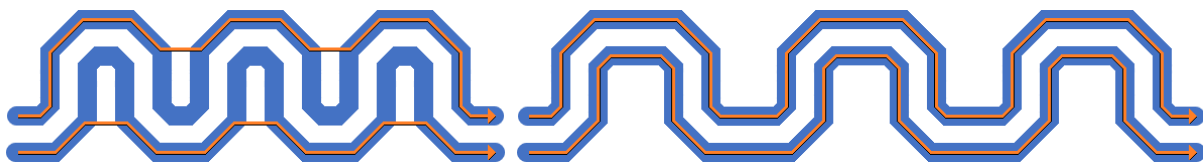
Figure 12.2: Differential Pair Clearance Inadequate, and Then Good When Spread
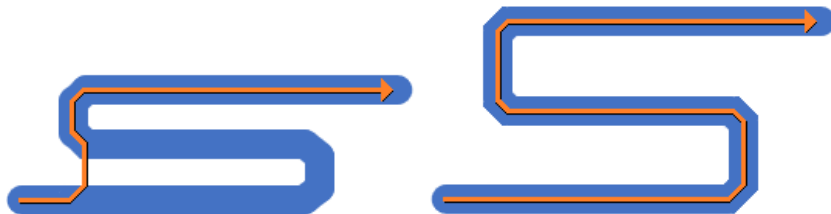
Figure 12.3: Trombone Tuning Clearance Inadequate, and Then Good When Spread

These conditions apply to ALL nets that are being tuned since only critical nets require tuning adjustments. If tuning is required, then the clearance needs to be sufficient to avoid significant same net coupling.

Same Net Clearance Based on Multiple of Height from Reference Plane
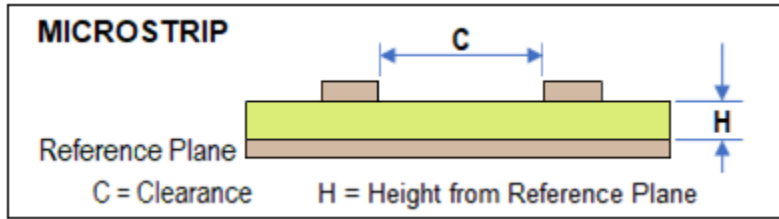
Figure 12.4: Same Net Coupling – Microstrip
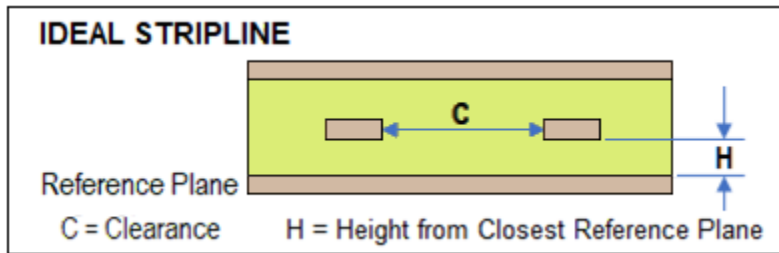
Figure 12.5: Same Net Coupling – Stripline

Crosstalk: Same Net - Height to Ref Plane				
	Microstrip		Stripline	
Edge Rate	Clearance			
	Effective Values	Extreme Values	Effective Values	Extreme Values
> 350 ps	3H	4H	2H	3H
< 350 ps	4H	5H	3H	4H
Clearance value based on the height (H) to reference plane				

Figure 12.6: Same Net Coupling Clearance – Height to Ref Plane

Same Net Clearance Based on Multiple of Trace Width – Limited Usefulness

Rick Hartley pointed out that using the trace width is only close to being accurate for 50 Ohm traces because their width is similar to the height to the reference plane.

For example, if the traces are 60 or 65 Ohms, the level of crosstalk will be much worse at 2 times trace spacing than at 2 times height above the plane. The reason is that 65 Ohm lines are narrower than 50 Ohm lines and their width is less than the height to the reference plane.
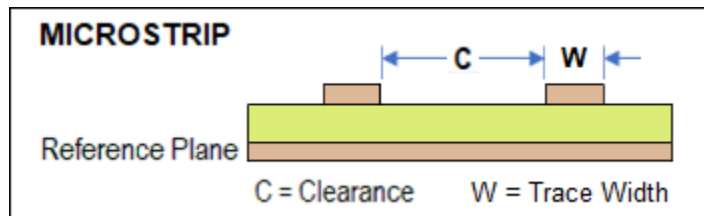
Figure 12.7: Same Net Coupling – Trace Width
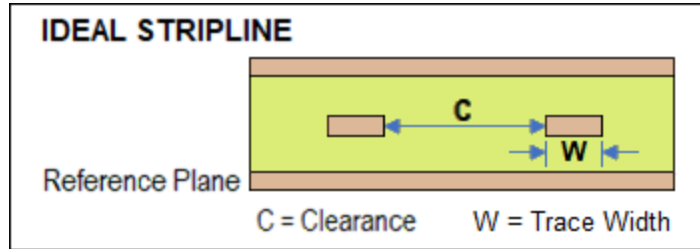
Figure 12.8: Same Net Coupling – Trace Width

Crosstalk: Same Net - Trace Width				
Edge Rate	Microstrip		Stripline	
	Clearance			
	Effective Values	Extreme Values	Effective Values	Extreme Values
> 350 ps	3W	4W	2W	3W
< 350 ps	4W	5W	3W	4W
Clearance value based on the trace width (W)				

Figure 12.9: Same Net Coupling Clearance – Trace Width

SOLUTION: The intent is to minimize the percent of energy coupling.

1. **Same Net Clearance Constraints**: Create the same net clearance constraints with adequate clearance (based on the distance to reference plane) for nets greater than critical length, as stated in Chapter 2.

2. **Reference Planes, Termination, Impedance**: See the Introduction to properly address these issues as they are essential for critical length nets.

3. **Routing Techniques**: If the ECAD system does not have the same net rule, spread the tuning segments according to the charts above.

4. **Simulation**: To ensure the same net crosstalk effects are sufficiently mitigated, simulate all the nets with tuning.

CHAPTER 13

Vias: Impedance

CONCERN: With high-speed nets, if the via impedance is not matched (within 10%) with the routing, the discontinuity can cause insertion loss and reflections that may significantly degrade signal quality.

- If the total interconnect length of the net is greater than its critical length, matching impedance for the via and trace is necessary.
  - Total interconnect length includes pin-package, routing, and via-used lengths.

SOLUTION:

1. **Calculate Via Impedance**: Use the excellent Saturn PCB Toolkit.[1]

Figure 13.1 Saturn PCB Toolkit

2. **Via Templates**: Create via templates that provide desired impedance for use when routing. Always work with your fabricator to understand which via sizes they support.

3. **Termination**: Properly terminate the signal to reduce or eliminate reflections.

4. **Simulation**: For nets that exceed the critical length, simulate to determine if the difference in via impedance compared to the track is significant (>10%) and modify via size as necessary to mitigate the potential problems.

5. **Deeper Analysis**: To do more thorough analysis of via impedance there are other tools that will likely provide that capability.

Polar Instruments
   https://www.polarinstruments.com/support/si/AP8178.html

Simberian
   Article: https://www.simberian.com/AppNotes/DesigningLocalizableMinimalReflectionVias_2009_05i.pdf

   Video: How to Build 3D EM Via-hole models for differential links:
   https://www.youtube.com/watch?v=T6LsSspcc-M&feature=youtu.be

Sci-Soft
   Article: https://www.sisoft.com/blog/posts/understanding-via-impedance.html
   Home page: https://www.sisoft.com/

References

1) Saturn PCB Toolkit, http://saturnpcb.com/pcb_toolkit/
2) Donald Telian, "Via Impedance,"
   https://www.sisoft.com/blog/posts/understanding-via-impedance.html
3) Yuriy Shlepnev, "Building Advanced Transmission Line and Via-Hole Models,"
   https://www.simberian.com/Presentations/Shlepnev_DesignCon_IBIS_Summit2008.pdf
4) Keysight, "Demystifying Vias in High-Speed PCB Design,"
   https://www.youtube.com/watch?v=FVKOC8xz1F0&ab_channel=KeysightDesignSoftware

CHAPTER 14

Vias: Plane Anti-Pad Size

CONCERN: The size of the plane anti-pad affects the via impedance and capacitance. Increasing the anti-pad clearance to the via pad in a plane reduces the capacitive effects of the via and the overall insertion loss, but it also increases the impedance.

- If the total interconnect length of the net is greater than its critical length, managing the anti-pad size is necessary.
  - o Total interconnect length includes pin-package, routing, and via-used lengths.

SOLUTION:

1. **Calculate Anti-Pad Size**: Use the Saturn PCB Toolkit to calculate the appropriate anti-pad size (Ref Plane Opening) while still maintaining the desired impedance.[1]

Figure 14.1: Saturn PCB Toolkit – Ref Plane Opening

2. **Create Anti-Pads**: The anti-pads are created either in the via pad stackup or indirectly by a plane clearance rule, depending on the ECAD system. Use the value that Saturn PCB calculates for the desired impedance and ask your fabricator if they will support that value. It may be too small for their fab process.

3. **Nonfunctional Pads**: If the via has nonfunctional pads removed, the plane anti-pad clearance should be applied to the hole. Work with your fabricator to get the appropriate anti-pad oversize for the hole.

4. **Anti-Pad Arrays**: Be aware of the potential for an array of the via anti-pads to block the return path in a plane. If this occurs, spread the vias to ensure an adequate and direct path through the array.

   If spreading is not feasible and the return path blockage must be removed, see if the anti-pad size can be effectively reduced. Work with your fabricator to define the oversize of the anti-pads.
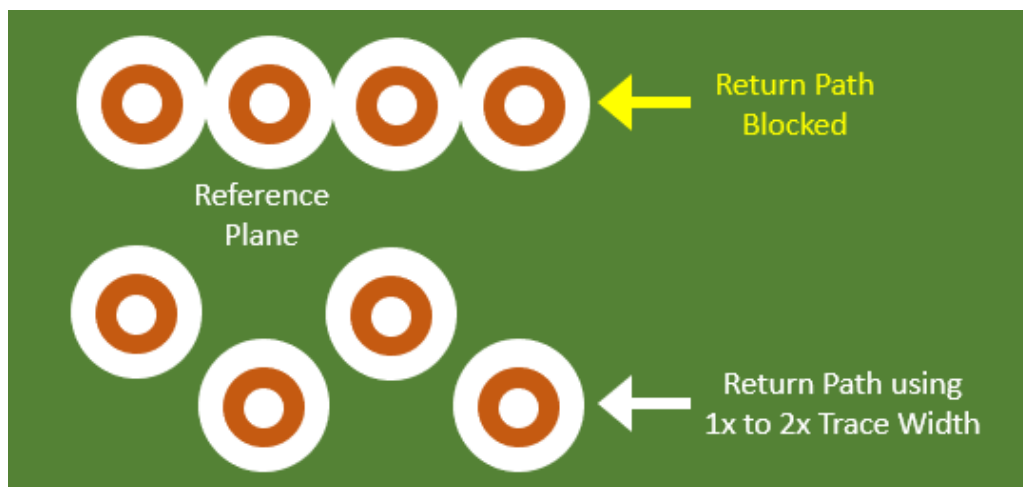
Figure 14.2: Move Vias
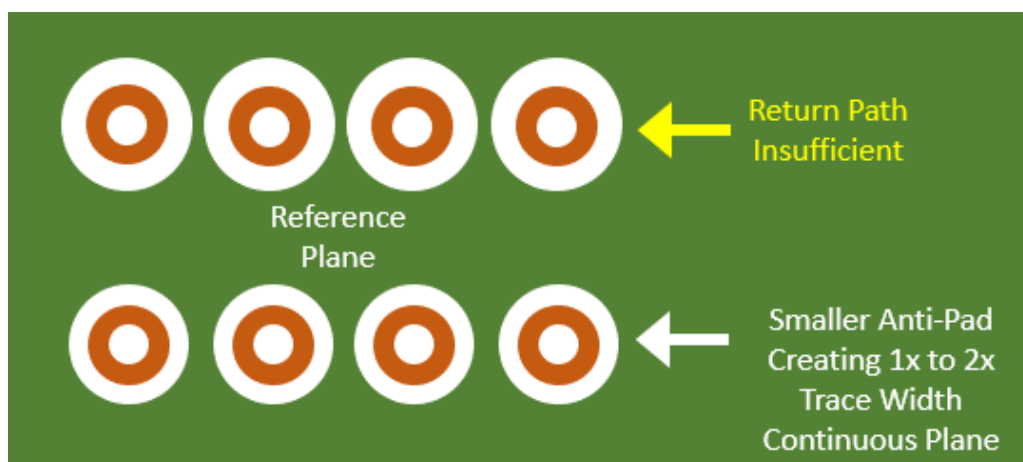
Figure 14.3: Make Anti-Pad Smaller

If you make smaller anti-pads for the array, verify the desired impedance.

5. **Oblong Anti-Pads**: Creating sufficiently sized anti-pad diameter is sometimes not feasible due to lack of space; however, an oblong shape can reduce parasitic capacitance significantly and still allow the return current to flow between the vias in a row or array.[2]

References

1) Saturn PCB Toolkit, http://saturnpcb.com/pcb_toolkit/
2) Barry Olney, "How to Handle the Dreaded Danglers, Part 2", The PCB Design Magazine, September 2016, page 34, http://iconnect007.uberflip.com/i/726276-pcbd-sept2016/31?m4=

CHAPTER 15

Vias: Stubs

CONCERN: At very-high edge rates, a via stub can create an antenna that causes insertion loss and the potential for noise that can degrade the signal or other signals.

- If the total interconnect length of net is greater than its critical length, via stubs create problems that must be mitigated.
  - Total interconnect length includes pin-package, routing, and via-used lengths.

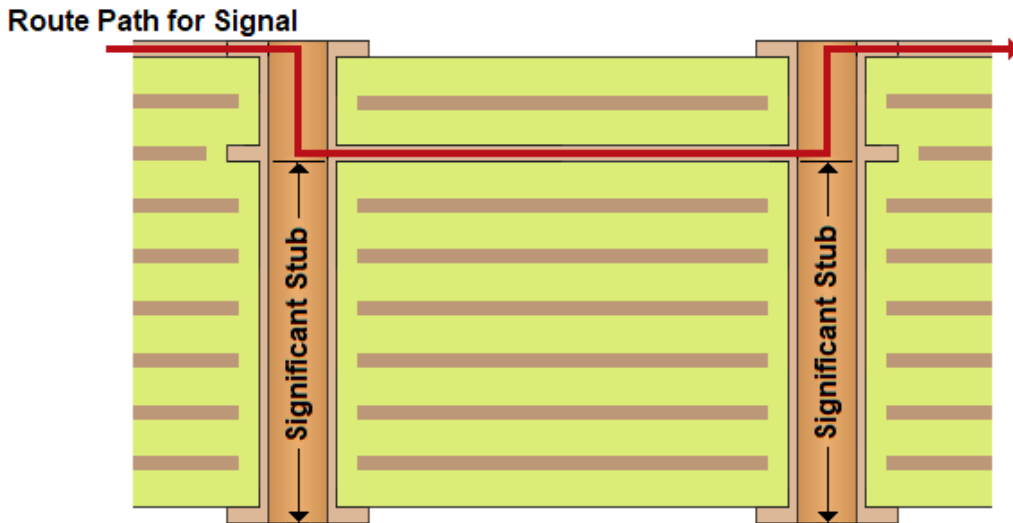- Create max stub length constraints for nets exceeding their critical length.

Figure 15.1: Example of Significant Via Stubs

Vias: Stub Length				
Edge Rate	English Units		Metric Units	
	Max Via Stub Length			
	Effective Values	Extreme Values (2/3)	Effective Values	Extreme Values (2/3)
200 ps	429 mil	286 mil	10.89 mm	7.26 mm
100 ps	214 mil	143 mil	5.44 mm	3.63 mm
80 ps	171 mil	114 mil	4.35 mm	2.90 mm
60 ps	129 mil	86 mil	3.27 mm	2.18 mm
40 ps	86 mil	57 mil	2.18 mm	1.45 mm
20 ps	43 mil	29 mil	1.09 mm	0.73 mm
10 ps	21 mil	14 mil	0.54 mm	0.36 mm

Figure 15.2: Max Via Stub Lengths

Decision Tree: Check to see if the max stub length in the chart is greater than the board thickness, or if the board only has 2 layers, or if only staggered uVias are used. If any of these conditions exist, no rule is needed. Layout Solutions are ordered by preference as related to effectiveness and cost.
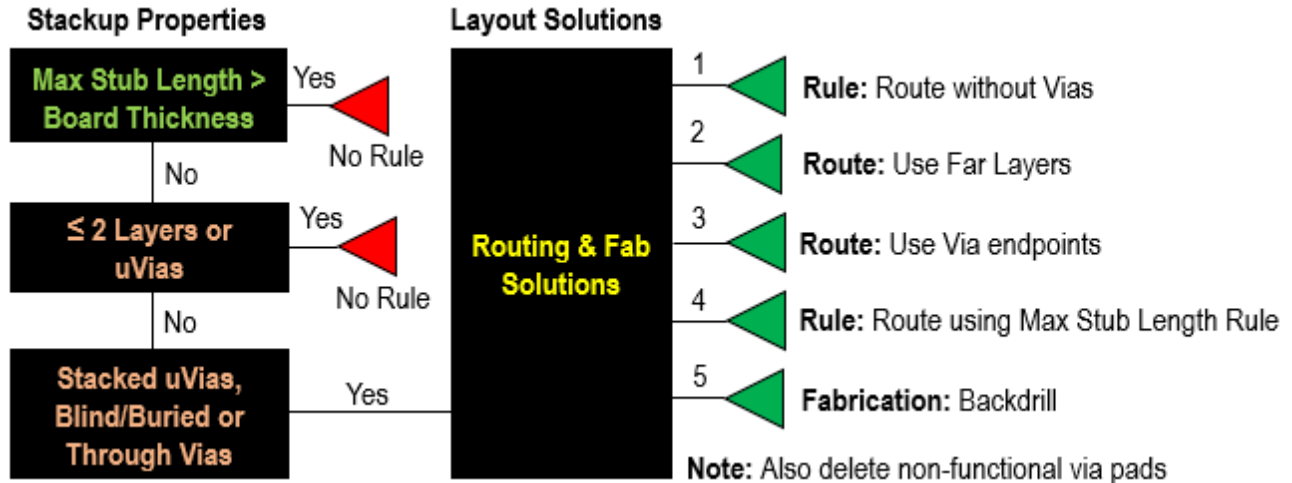
SOLUTIONS:

Figure 15.3: Decision Tree for Via Stub Solutions

1. **Route Without Vias**: Set max via count constraint to zero.

   - Although it is not practical to do this on a significant digital layout, routing the signals with the fastest edge rate on the outer layers without vias is an excellent method. Make sure effective reference planes are adjacent to the outer layers or the routes are shielded with as described in Chapter 4.

2. **Route Between Far Layers**: Route critical nets between layers far enough apart that a significant via stub is eliminated.
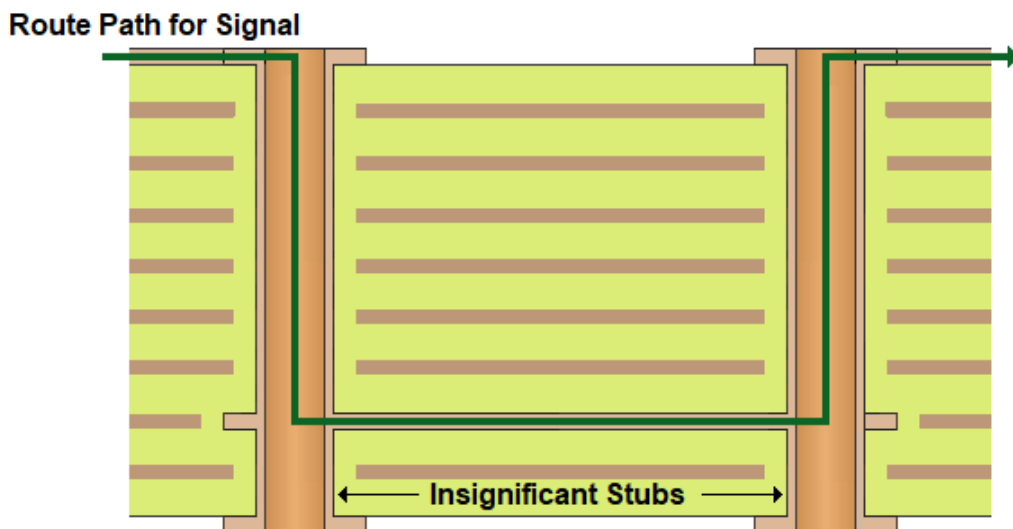
Figure 15.4: Far Layer Routing to Eliminate Significant Via Stubs

- When routing between far layers, make sure critical nets are routed on a layer adjacent to an effective reference plane. Plus, stitch vias may be needed to connect the planes as described in Chapter 5.

3. **Route Using Via Endpoints**: Eliminates via stubs all together

   - Blind/buried vias and μVias – Opportunity for truly short via lengths.

   - Through-hole vias – Route using outer layers only.

4. **Back Drill in Fabrication**: Use the max via stub Length constraint.

   - This will increase the cost. Work with the fabricator to determine the oversized diameter and the depth values which vary based on the fabricator's equipment and process.

   - If you are removing nonfunctional pads, make sure the anti-pads on plane layers are large enough and any traces on signal layers are far enough away to clear the drill hole.

Route Path for Signal
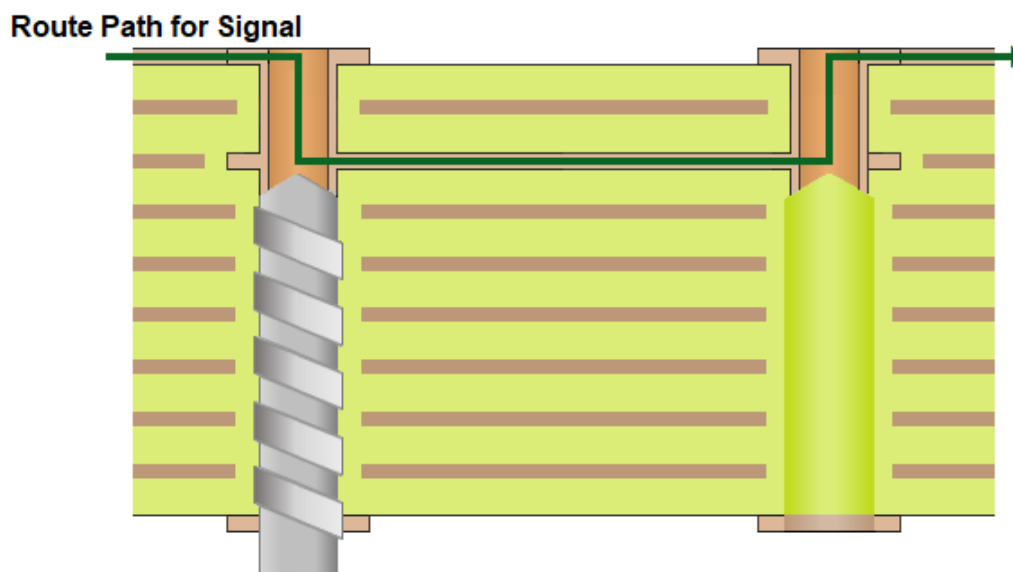
Figure 15.5 Backdrilling

Equations

To determine the max stub length, the Bogatin Rules of Thumb equations in "How Long a Stub is Too Long"[1] and "What is the Bandwidth of a High- Seed Serial Link Signal?"[2] are used.

BR = Bit rate (same as data rate, if it is not multiplied as with DDR or QDR)

$$\text{Length[in]} < \frac{0.3}{BR\text{[Gbps]}}$$

To calculate the bit rate from the rise time,

$$BR\,[\text{ps}] = \frac{140}{Tr[\text{ps}]}$$

$$\text{Length[in]} < \frac{0.3}{140/Tr[\text{ps}]} \qquad \text{Length[mil]} < \frac{300}{140/Tr[\text{ps}]}$$

References

1) Eric Bogatin, Rule of Thumb #18, "How Long a Stub is Too Long?"
   https://www.colorado.edu/faculty/bogatin/rules-thumb
2) Eric Bogatin, Rule of Thumb # 11, "What is the Bandwidth of a High-Speed Serial-Link Signal?"
   https://www.colorado.edu/faculty/bogatin/rules-thumb
3) Bert Simonovich, "Via Stubs Demystified,"
   https://blog.lamsimenterprises.com/2017/03/08/via-stubs-demystified/

CHAPTER 16

Vias: Nonfunctional Pads

CONCERN: When vias are used in the routing of very high-speed signals, the nonfunctional pads (unconnected pads) can contribute to noise radiation. This chapter also applies to through-hole pins.

Although there is much debate in the literature as to the pros and cons of nonfunctional pad removal, if the fabricator supports this method, it can be used to improve signal integrity. For example, removing the nonfunctional pads increases the impedance, which could help to match the trace impedance.

- If the total interconnect length of the net is greater than its critical length, removing nonfunctional pads will significantly reduce noise radiation.
  - o Total interconnect length includes pin-package, routing, and via-used lengths.

SOLUTION:

1. **Fabricator Capabilities**: Check your fabricator to ensure they support the removal of nonfunctional pads. Some fabricators like to keep the pads, some don't.[1]

2. **Outer Layers**: Preserve pads on the start and end layers. Most fabricators don't recommend removing pads on outer layers.

3. **Layout Completed**: If nonfunctional pads are to be removed, use the pad removal routine after the layout is completed to ensure all are removed.
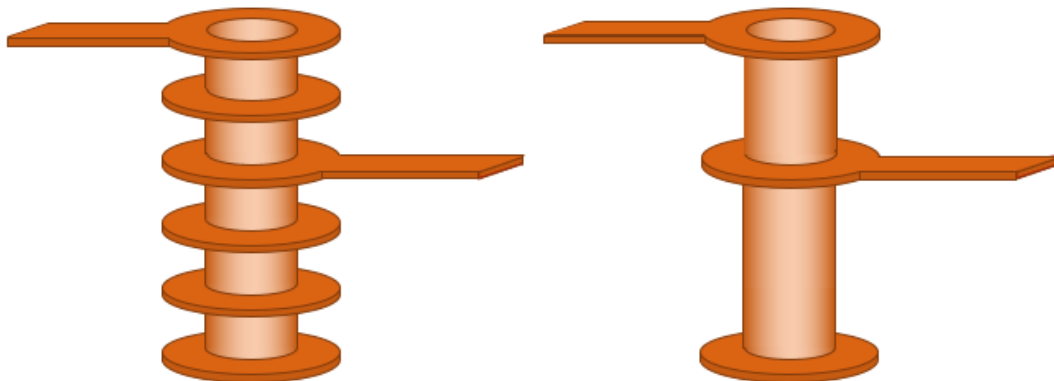

Figure 16.1: Via Before/After Nonfunctional Pads Removed

4. **Increasing Routing Space**: Occasionally, the removal of nonfunctional pads is necessary to provide extra room for routing between the vias or pins, as is the case with some through-pin connectors. In this case, the pads should be removed as the routing requires.

5. **Copper Pour Areas**: Removing nonfunctional pads can also increase the copper pour area on planes.[1]

6. **Landless Vias**: An alternative approach would be to use landless vias.[2]

References

1) Mark Hughes, "Use It or Lose It? What Should You Do with Nonfunctional Pads?" https://www.allaboutcircuits.com/technical-articles/use-it-or-lose-it-what-should-you-do-with-non-functional-pads/

2) Happy Holden, "Landless Vias," https://resources.altium.com/pcb-design-blog/landless-vias

CHAPTER 17

Vias: Differential Pair Via-Via Spacing

CONCERN: When vias are used for the differential pair complements, locate them as close as possible edge-to-edge, without violating the fabrication minimum clearance. If they are spread too far apart it will affect the impedance of the differential signal (Zdiff), which can cause reflections that degrade the signal. Tight coupling of the differential pair vias could also make the impact of crosstalk less.[1]

- If the total interconnect length for the differential pair is greater than its critical length, a via-via max spacing is needed for impedance management.
  - Total interconnect length includes pin-package, routing, and via-used lengths.

This rule may be difficult to fulfill when doing a fanout of a pin-array type component such as a BGA or connector since the fanouts must be spread due to the pin array pitch.

SOLUTION: A via-via max spacing rule can be used; however, not all ECAD systems have this rule. A good approach is to make the minimum space between the complement vias the same as the differential pair gap and place the vias at that minimum spacing and use teardrops as shown in the figure below.
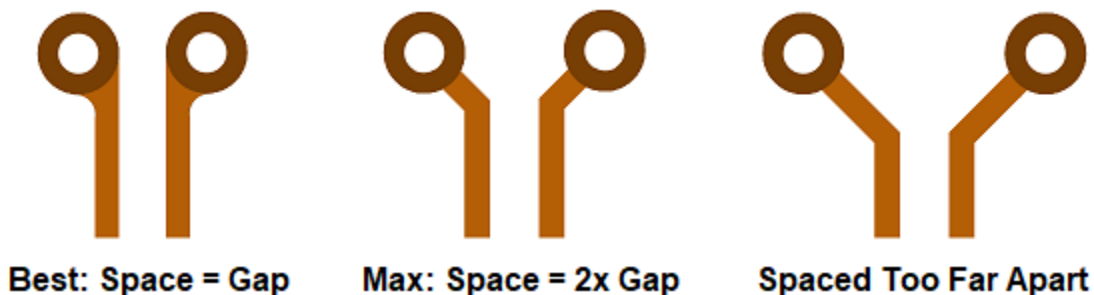

Figure 17.1: Differential Pair Via Spacing

For critical length differential pairs, the best via-via spacing is equal to the gap between the complements. Otherwise, the maximum spacing should be 2x the gap.

References

1) Heesoo Lee, "Demystifying Vias in High-Speed PCB Design," page 26, https://docplayer.net/55471200-Demystifying-vias-in-high-speed-pcb-design.html

CHAPTER 18

Routing: Trace Stubs

CONCERN: Trace stubs can have a significant effect on signal integrity if they are too long. They can behave like an antenna, causing insertion loss and the potential for noise that can degrade the signal and cause errors.

The most common example of the need to eliminate trace stubs is with the address and control lines in DDR memory circuits that use fly-by technology.

A trace stub is formed when a multipin net is routed with T-branches or when there is a branch for a test point or some instance in which there is not direct point-to-point routing.[1]

- If the total interconnect length of the net is greater than its critical length, trace stubs are a problem that needs mitigation.
    - Total interconnect length includes pin-package, routing, and via-used lengths.

- For nets exceeding their critical length, calculate the max length for trace stubs.

	English Units		Metric Units	
Edge Rate	**Max Trace Stub Length**			
	Effective Values	**Extreme Values (2/3)**	**Effective Values**	**Extreme Values (2/3)**
1 ns	2.14 in	1.43 in	54.43 mm	36.29 mm
700 ps	1.50 in	1.00 in	38.10 mm	25.40 mm
500 ps	1.07 in	714 mil	27.21 mm	18.14 mm
400 ps	857 mil	571 mil	21.77 mm	14.51 mm
300 ps	643 mil	429 mil	16.33 mm	10.89 mm
200 ps	429 mil	286 mil	10.89 mm	7.26 mm
100 ps	214 mil	143 mil	5.44 mm	3.63 mm
80 ps	171 mil	114 mil	4.35 mm	2.90 mm
60 ps	129 mil	86 mil	3.27 mm	2.18 mm
40 ps	86 mil	57 mil	2.18 mm	1.45 mm
20 ps	43 mil	29 mil	1.09 mm	0.73 mm
10 ps	21 mil	14 mil	0.54 mm	0.36 mm

Table title: Routing: Trace Stub Length

Figure 18.1: Max Trace Stub Length

SOLUTION:

1. **Create Max Trace Stub Length Constraints**: Set constraint values based on edge rate as described in Chapter 2.

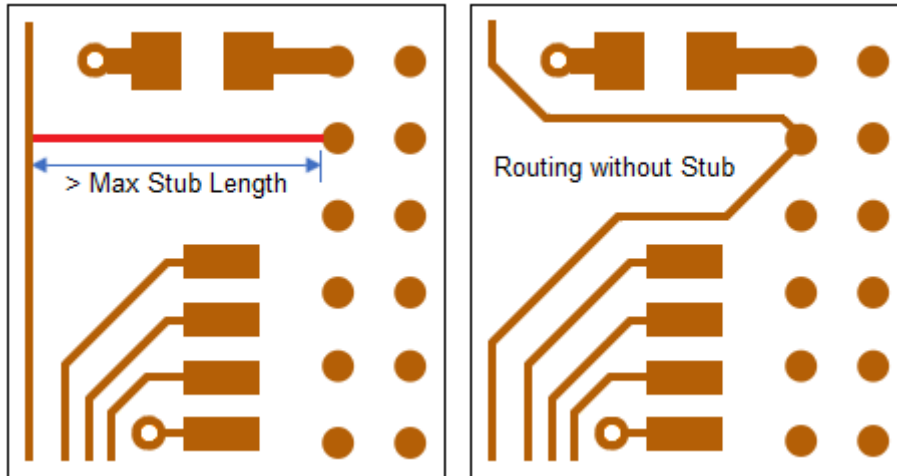2. **Route Point-to-Point**: Use point-to-point routing to eliminate long stubs.

Figure 18.2: Trace Stub Example

Equations

The max stub length equations are from the Bogatin Rules of Thumb in "How Long a Stub is Too Long"[1] and "What is the Bandwidth of a High-Speed Serial Link Signal?"[2]

BR = Bit rate (same as data rate, if it is not multiplied as in DDR or QDR)

$$\text{Length[in]} < \frac{0.3}{BR[\text{Gbps}]}$$

To calculate the bit rate from the rise time, $BR\,[\text{ps}] = \dfrac{140}{Tr[\text{ps}]}$

$$\text{Length[in]} < \frac{0.3}{140/Tr[\text{ps}]} \qquad \text{Length[mil]} < \frac{300}{140/Tr[\text{ps}]}$$

References

1) Eric Bogatin, Rule of Thumb #18, "How Long a Stub is Too Long?"
   https://www.colorado.edu/faculty/bogatin/rules-thumb
2) Eric Bogatin, Rule of Thumb # 11, "What is the Bandwidth of a High-Speed Serial-Link Signal?"
   https://www.colorado.edu/faculty/bogatin/rules-thumb

CHAPTER 19

Routing: Trace Corners

CONCERN: For critical length nets, does it matter if trace corners are 45°, arcs or square? One engineer appropriately said, "Over 16 Gbps, everything matters." Yet, many high-speed experts have done the simulations and concluded that unless you are doing RF or analog, the corners have an insignificant impact on signal loss or impedance.[1]

Figure 19.1: Trace Corners

SOLUTIONS:

1. **45° Corners**: This is the most common corner and ECAD systems are developed to fully support adding and editing them. Their big advantage over square corners is shorter routing paths and the ability to meander through tight areas.

2. **Arc Corners**: How well does the ECAD system support the addition and editing of arcs? Does it support concentric arcs and allow them to be pushed and shoved with perfect results. Can the radius be easily changed? What does gloss do to them? When they are dragged, do they behave as expected? If arcs are easy to edit there isn't any reason not to use them. Arcs are necessary with flex designs to mitigate the possibility of the route cracking when flexed.

3. **Square Corners**: Even if they are not a problem for "normal" high-speed design, they are not efficient in a dense routing area and they are more difficult to edit.

4. **Any-Angle Routing**: Some ECAD systems support any-angle routing. It can be useful when doing flex and squeezing into places that 45° traces won't fit like through fine-pitch BGAs. If adding and editing functions for any-angle traces easy and automated, any disadvantages are eliminated.

References

1) Eric Bogatin, Rule of Thumb #24, "When to Worry about Trace Corners?"
   https://www.colorado.edu/faculty/bogatin/rules-thumb

CHAPTER 20

Routing: Differential Pair Split

CONCERN: When routing tightly coupled differential pairs and they split around objects, an impedance discontinuity is created and there is the potential for imbalanced EMI effects on the differential pair complements.

- If the total interconnect length for the differential pair is greater than its critical length, splitting differential pairs around objects needs to be avoided if possible.
  - Total interconnect length includes pin-package, routing, and via-used lengths.

SOLUTIONS:

1. **BGAs**: Avoid splitting any critical length differential pairs; however, splitting the complements may be necessary when escaping very fine-pitch BGAs.

2. **Impedance**: If the complements must be split inside a BGA, change the width of the traces in that area to more closely match the impedance of the tightly coupled differential pair routing. The split traces should have an individual impedance half the value of the differential impedance, Zo = Zdiff/2.

3. **1mm Pitch BGAs**: When escaping 1mm pitch BGAs, if the differential pairs trace width and gap is 0.1mm, it does not need to be split, assuming the via-pad sizes and clearances are set up appropriately. For example, try using a 0.1mm grid.[1]
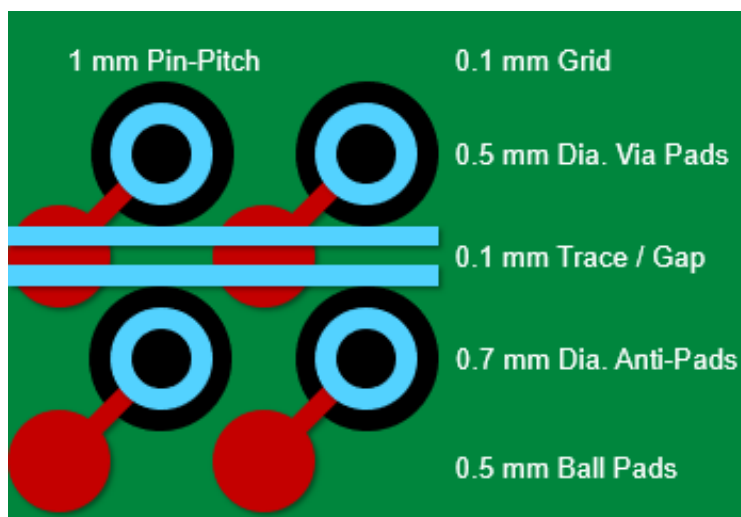
Figure 20.1: Differential Pair Routing in 1mm BGA

- There is a potential problem with this approach: The traces are on the edge of the anti-pads which could cause an impedance discontinuity as described in Chapter 4.

4. **Splitting Outside BGAs**: When routing outside BGAs, it is best to avoid splitting whenever possible. Some ECAD systems have a rule for max uncoupled length. Set this to "0" and then any instance will be flagged.
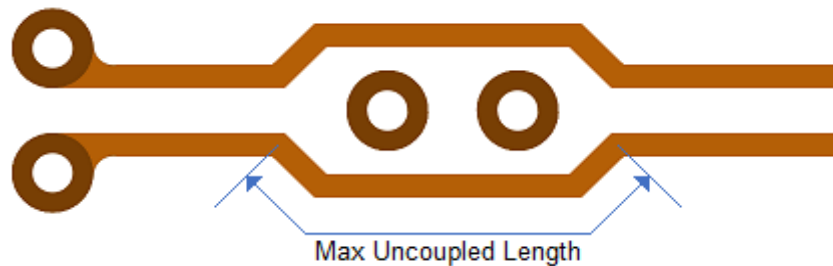   - It may be possible to create a rule area that allows splitting inside very-fine pitch BGAs.

Figure 20.2: Differential Pair Max Split Rule

5. **Simulation**: To ensure when splitting or changing trace widths and clearances the impedance discontinuities are kept insignificant simulate the differential pairs.

References

1) Michael R. Creeden, "PCB Design Best Practices," page 19, https://www.altium.com/live-conference/sites/default/files/pdf/PCB%20Design%20Best%20Practices_%20Routing%20Techniques%20in%20Altium%20Designer%20-%20Mike%20Creeden.pdf

Routing: Length Match Methods

Adding length to routes can be accomplished by using accordion, trombone, notched or wacko patterns.

Single-Ended Nets

Accordion

This is the most common pattern. An irregular pattern is useful when having to get around vias and to avoid crosstalk from other nets. Round or 45° degree corners are good. This pattern is also called a serpentine pattern.

For critical length nets, it is important to have a gap between the segments wide enough to avoid the same net crosstalk as defined in Chapter 12.

Figure 21.1: Regular and Irregular Patterns

Trombone

The length compared to the accordion pattern is about the same depending on the shape of the corners and the number of them.

For critical length nets, the gap between the segments has to be wide enough to avoid the same net crosstalk. It also more likely that a trombone pattern would exceed critical parallel length with another net and be susceptible to crosstalk.

Figure 21.2: Trombone Pattern

Notched

The notched pattern is useful to avoid the same net crosstalk. It doesn't add much length (only the added length of angled lines as compared to a straight line), but for slight adjustments, it is particularly good.

Figure 21.3: Notched Pattern

Wacko

For lack of a better word, I will call patterns like this "Wacko." I doubt a designer would add length like this with manual tuning, but I certainly have seen automatic tuning routines do this. The biggest problem is effectively editing them. It is easier to delete and re-do it with a more conventional irregular pattern.
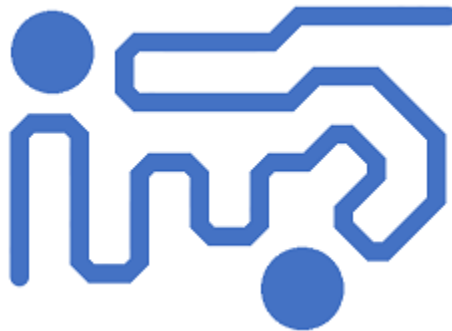
Figure 21.4: Wacko Pattern

Differential Pairs

Tuning differential pairs to a group matched length has the same concerns as single-ended nets to avoid the same net crosstalk as described in Chapter 12.
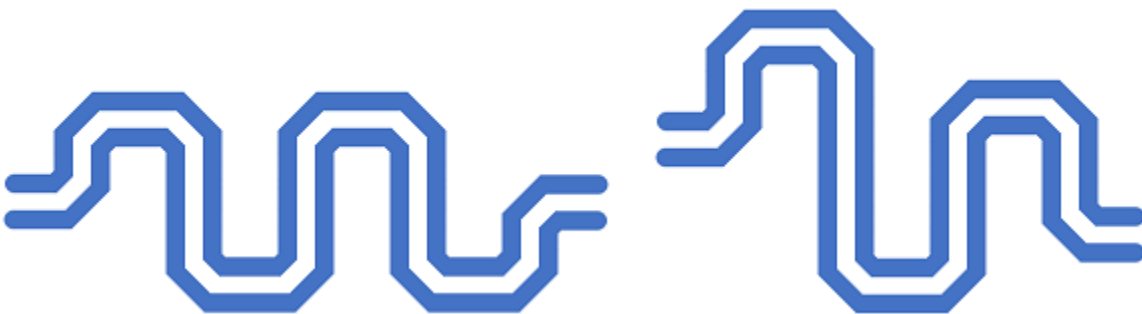
Figure 21.5: Differential Pair Regular and Irregular Patterns

There can be additional problems related to tuning of individual complements of the differential pair for within-pair length matching or phase matching as described in Chapters 6 and 9.

Angled Tuning Bumps

When adding tuning bumps (also called phase bumps) to an individual differential pair compliment, the common style is one with angled lines. However, if the tuning bumps separate the differential pair complements more than 2x differential pair gap, or the length of the segment is more than 3x the trace width, there can be a significant impedance discontinuity.
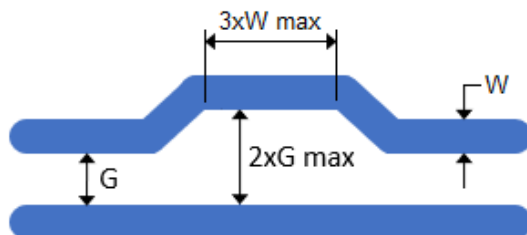

Figure 21.6: Max Spacing of Tuning Bumps

With this type of tuning bump, the only length added is with the angled lines (as compared to a straight line) and as such, to add significant length it requires a large number of them.

With 45°bumps, each angled line is about 41% longer than the straight line, according to Mr. Pythagoras. For example, if the height of the bump is 5 mils, the angled line will add 2.1 mils to the overall length of the route.

Extended Tuning Bumps

If the tuning bumps need to add significant length and the method in Figure 21.6 isn't adequate, Figure 21.7 shows the type of bump that can be used. However, the distance between the two parallel lines needs a minimum clearance of 2x the differential pair gap to prevent same-net crosstalk on very high-speed nets, which can make the added length ineffective. See Chapter 12 for more accurate same net clearance based on edge rate.
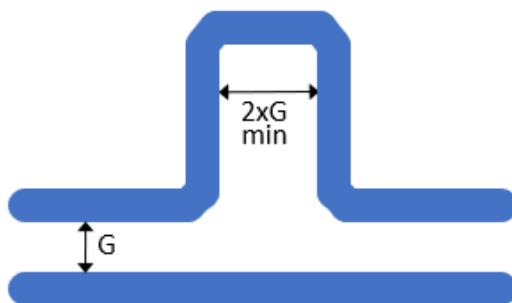

Figure 21.7: Avoid Same-Net Crosstalk

There is an impedance discontinuity created with the separation of the complements. Simulate to determine if it is significant.

Interesting Reference

Intel published, "AN 875: Intel Stratix 10 E-Tile PCB Design Guidelines," starting on page 19, which describes how to manage crosstalk and impedance problems with a 56Gbps channel. It suggests increasing the width of the traces when adding tuning patterns to improve impedance matching.

https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/an/an875.pdf

Below is a figure from the Intel document:

Figure 21.8: Intel Trace De-Skew Trombone Configuration

Chapter 22

Conclusion

This book has been an endeavor of researching the best practices in our industry and using my design experience, along with working in the ECAD software industry, mostly with Mentor Graphics, and then Altium. I intend to clearly provide constraint values and methods to solve the routing problems of high-speed design without over-constraining.

I hope you will find it useful and that it will help you create better-performing designs in less time.

For questions and comments:

Send an email to Charles Pfeil:

PCBconstraints@gmail.com